Timers and Counters in PLC

B.Tech. : Mechanical Engineering,
Year/Semester: III / V
Subject: Mechatronic Systems (5ME3-01)

By:
Praveen Saraswat
Associate Professor
Department of Mechanical Engineeing
Swami Keshvanand Institute of Technology, Management & Gramothan, Jaipur

Lecture Outcomes

The students will be able to:

- **Understand the concept of timers and counters in PLC controller.**

- **Apply timers and counters functions in ladder logic applications.**

Introduction

• Timers

- A timer is a PLC instruction measuring the amount of time elapsed following an event.

- Timer instructions come in two basic types: on-delay timers and off-delay timers. Both “on-delay” and “off-delay” timer instructions have single inputs triggering the timed function.

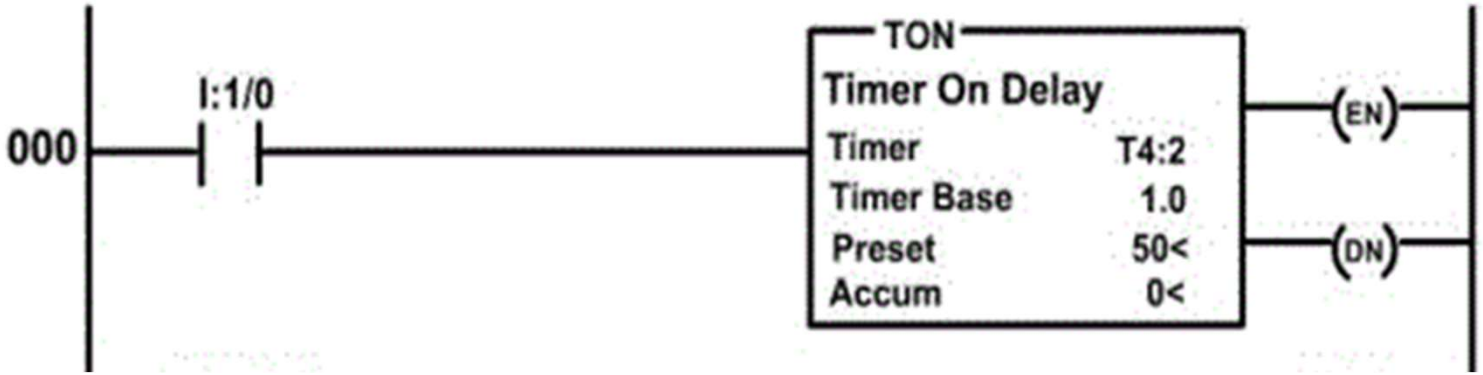
- The accuracy and repeatability of the timer are extremely high because the PLC processor generates delays.

- A timer starts counting at time-based intervals and continues until the accumulated value equals the preset value.

- **Timers are used to delay actions**
  - **Keep an output on for a specified time after an input turns off**
  - **Keep an output off for a specified time before it turns on**
- **Timing functions are vital in PLC applications**
  - **Cycle times are critical in many processes**
- **Many PLCs use block-type timers and counters**
  - **Compliance with IEC 61131-3 standards**

Timer Attributes

- Timer
- Time Base
- Preset
- Accumulator



On Delay Timer

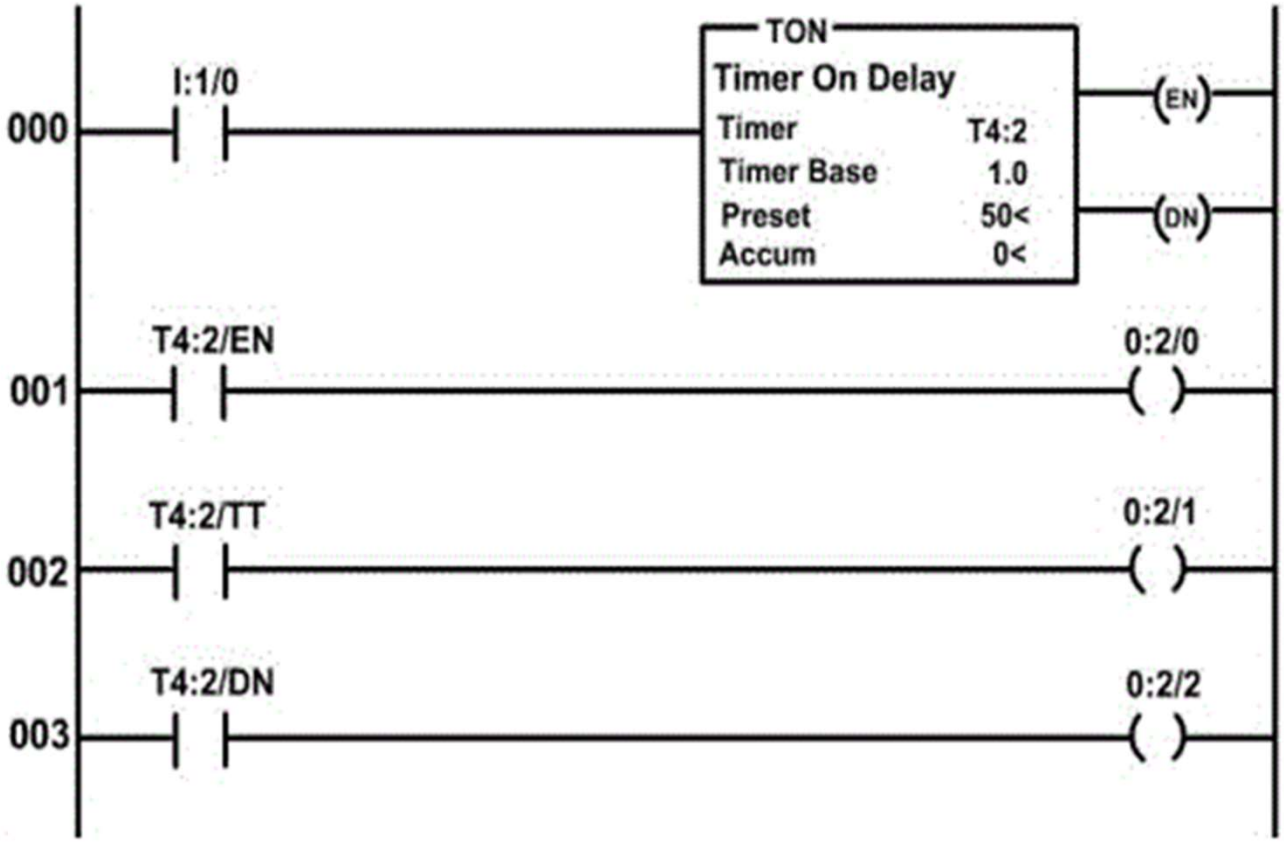
- An “on-delay” timer activates an output only when the input has been active for a minimum amount of time.
- The timer starts operating, when the rung is turned ON.
- When the rung is on, the timer starts counting until the preset value is equal to the accumulated value.
- The timer starts counting when the rung is turned ON, the counting of accumulated value will be shown at the ET rung on the timer logic.

Status Bits

- Timer Status bits can be used in ladder logic
- Status Bits (EN, DN, TT)

Bit	Set When	Remains Set Till
Timer done Bit (bit 13 or DN)	Accumulated value is equal to or greater than the preset value	Rung conditions go false
Timer Timing bit (bit 14 or TT)	Rung conditions are true and the accumulated value is less than the preset value	Rung conditions go false or when the done bit is set
Timer enable bit (bit 15 or EN)	Rung conditions are true	Rung conditions go false

TON Timer Ladder Diagram



Timer OFF Delay (TOF)

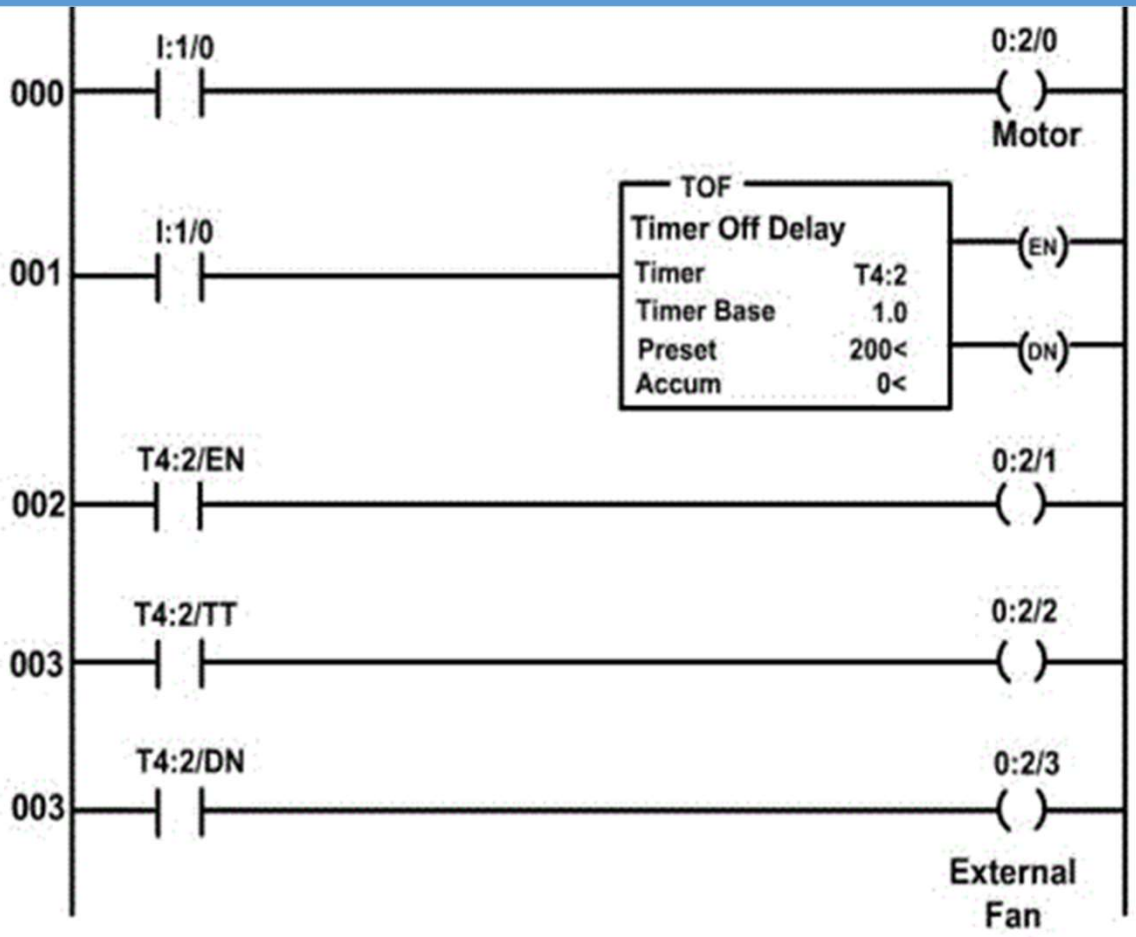
Used to turn an output On or OFF after rung has been off for a desired time:

- TOF starts to accumulate time when the rung becomes false
- It continues to accumulate time until the accumulated value equals the preset value or the rung becomes true
- The timer enable bit (EN bit 15) is set when the rung becomes true. It is reset when the rung becomes false and ACC < PRE or the DN bit is reset (ACC = PRE)
- The done bit (DN bit 13) is reset when the ACC value is equal to the PRE value. The DN bit is set when the rung becomes true

- **TOF Bits:**

Bit	Set When	Remains Set Till
Timer done Bit (bit 13 or DN)	Rung conditions are true	Rung conditions go false and the accumulated value is greater than or equal to the preset value
Timer Timing bit (bit 14 or TT)	Rung conditions are false and the accumulated value is less than the preset value	Rung conditions go true or when the done bit is reset
Timer enable bit (bit 15 or EN)	Rung conditions are true	Rung conditions go false

TOF Timer Ladder Logic



Retentive Timer On

- **RTO Instruction:**
  - Used to turn an output On after a set time period

1. The RTO timer is an accumulating timer. It retains the ACC value even if the rung goes false
   - To zero the ACC value, use a reset (RES) instruction in another rung with the same address as the RTO
2. The status bits can be used as contacts in the ladder diagram

Counters

- A counter is a simple device intended to do one simple thing-count. Every PLC has counter instructions.
- Counters usually use low-to-high transition from an input to trigger the counting action.
- Counters count the number of low-to-high transitions on the input line
  - Similar to Timers, which count the number of time increments
- Counters also have a reset instruction to clear the accumulated count

Count-up Counter (CTU)

The CTU is an instruction that counts false-to-true rung transitions.

- Rung transitions can be caused by events occurring in the program (from internal logic or by external devices) such as parts traveling past a detector or actuating a limit switch.

- The ability of the counter to detect false–to–true transitions depends on the speed (frequency) of the incoming signal.

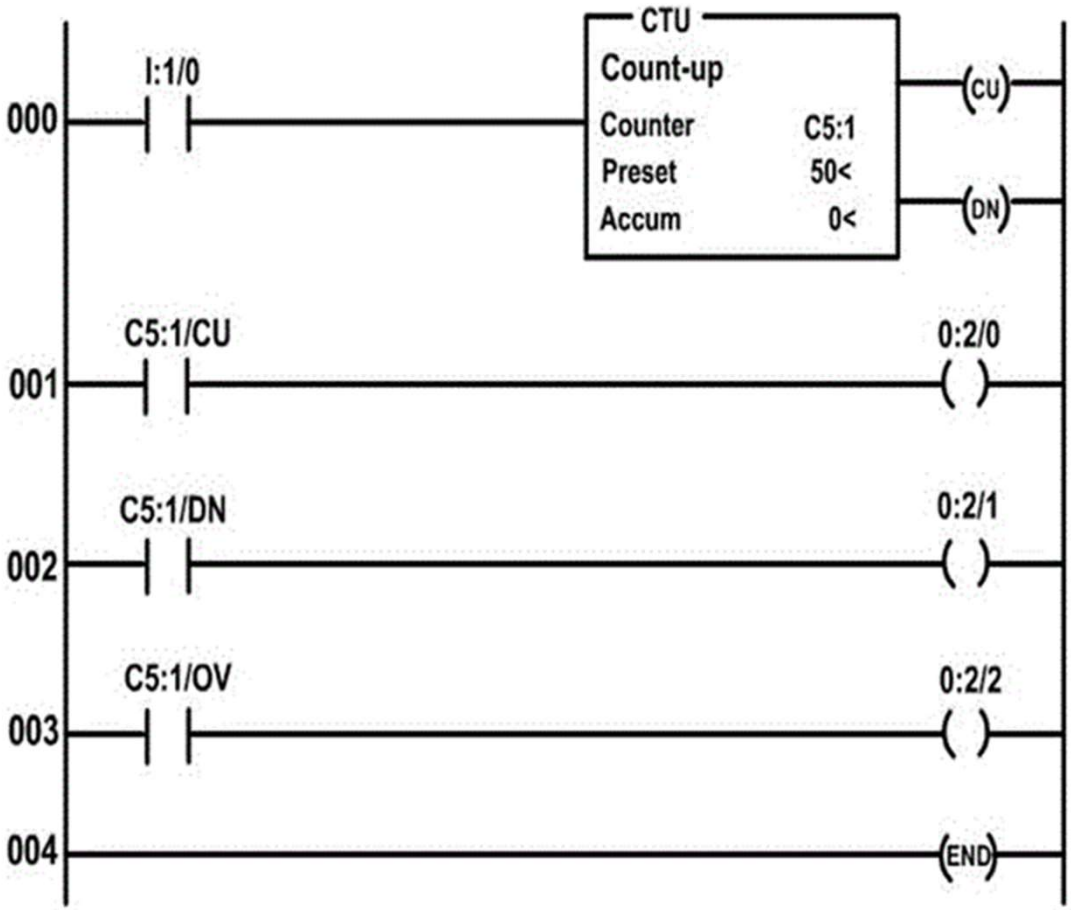
- The accumulated value is retained when the rung conditions again become false.

- The accumulated count is retained until cleared by a reset (RES) instruction.

CTU Counter Bits

Bit	Set When	Remains Set Till
Count-up Overflow bit (bit 12 or OV)	Accumulated value wraps around to -32,768 (from +32,767) and continues up from there towards zero	A RES instruction that has same address as the CTU instruction is executed or the count is decremented less than or equal to +32,767 with a CTD instruction
Done bit (bit 13 or DN)	The accumulated value is => the preset value	The accumulated value becomes less than the preset value
Count-up enable bit (bit 15 or CU)	Rung conditions are true	Rung conditions go false or a RES instruction that has the same address as the CTU instruction is enabled

Count-Up Counter Ladder Diagram



Count-Down Counter (CTD)

- The CTD is an instruction that counts false-to-true rung transitions.
- – Rung transitions can be caused by events occurring in the program such as parts traveling past a detector or actuating a limit switch.
- When rung conditions for a CTD instruction have made a false-to-true transition, the accumulated value is decremented by one count, provided that the rung containing the CTD instruction is evaluated between these transitions.

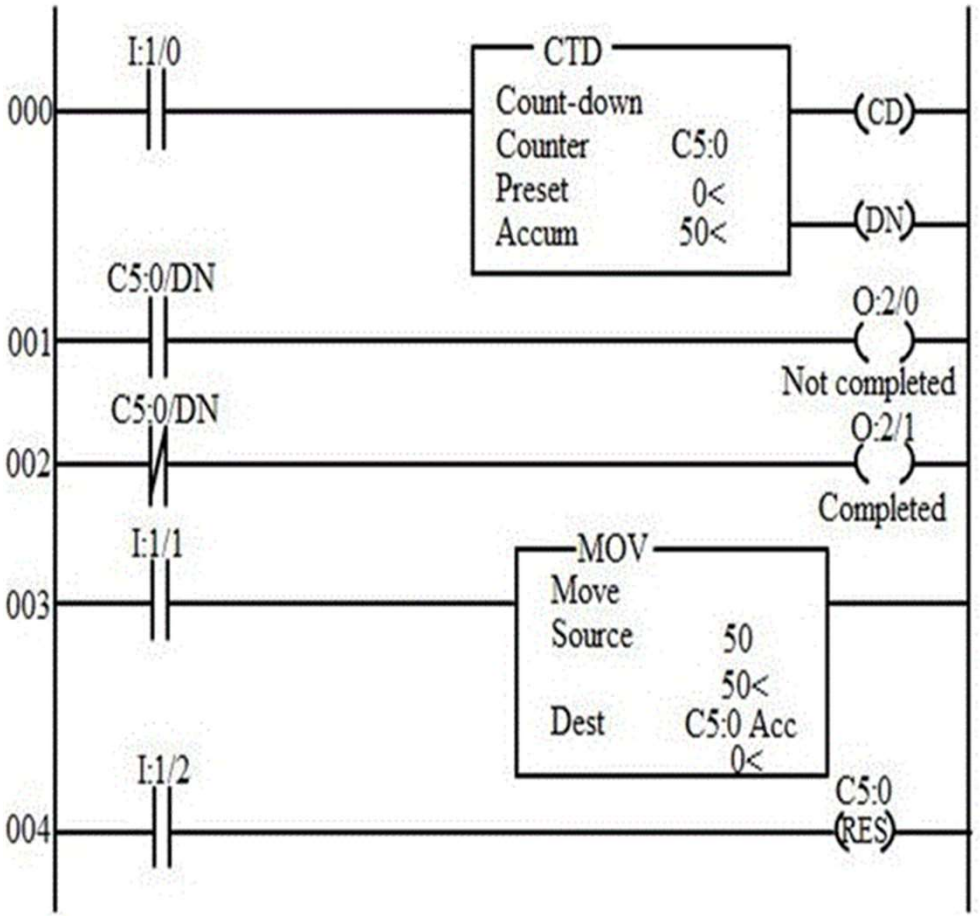
• The accumulated counts are retained when the rung conditions again become false.

The accumulated count is retained until cleared by a reset (RES) instruction.

CTD Counter Bits

Bit	Set When	Remains Set Till
Count-down Underflow bit (bit 11 or UN)	Accumulated value wraps around to +32,768 (from: -32,767) and continues counting from there	A RES instruction that has same address as the CTD instruction is executed or the count is incremented greater than or equal to +32,767 with a CTU instruction
Done bit (bit 13 or DN)	The accumulated value is ≥ the preset value	The accumulated value becomes less than the preset value
Count-down enable bit (bit 14 or CD)	Rung conditions are true	Rung conditions go false or a RES instruction that has the same address as the CTDinstruction is enabled

Count-Down Counter Ladder Diagram



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