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Synthesis of LUT Based Approximating Adder Circuits with Formal Error Guarantees

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Abstract

Approximate computing relaxes accuracy, enhance efficiency, and benefit in terms of area. It is widely popular in emerging applications like mining, search, vision, recognition where inaccuracies are tolerable. This tolerance towards errors is exploited to design circuits. The most crucial stage is to strike the proper balance between error and output quality. A systematic framework is used for generating approximate circuits with a specific error guarantee. The key idea is to use the property checking

technique based on SAT to compute the worst-case error. In this design method Look-up Table (LUT) is used to acquire approximation with worst-case error metric as a constraint. A novel technique is proposed to select nodes for insertion of LUTs is discussed. The method evolved around toggle count and observability of nodes in the circuit. The number of transistors used, and errors is examined for analysis. This analysis will help in evaluating the output of the adder circuit obtained through approximation. This method was implemented using Yosys and evaluated adder circuit. The aim of this paper is to adopt formal methods such as satiability solvers for analysis of approximate adder circuits. When the worst-case absolute error and area are taken into account for 64 bit, 32 bit and 16 bit our solution will provide a superior trade-off.

Keywords

SAT **Approximation** **LUT** **Adder circuits**

Approximate computing

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