



[International Symposium on VLSI Design and Test](#)
VDATE 2022: **VLSI Design and Test** pp 435–449

Synthesis of LUT Based Approximating Adder Circuits with Formal Error Guarantees

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Conference paper | [First Online: 17 December 2022](#)

251 Accesses

Part of the [Communications in Computer and Information Science](#) book series (CCIS, volume 1687)

Abstract

Approximate computing relaxes accuracy, enhance efficiency, and benefit in terms of area. It is widely popular in emerging applications like mining, search, vision, recognition where inaccuracies are tolerable. This tolerance towards errors is exploited to design circuits. The most crucial stage is to strike the proper balance between error and output quality. A systematic framework is used for generating approximate circuits with a specific error guarantee. The key idea is to use the property checking

technique based on SAT to compute the worst-case error. In this design method Look-up Table (LUT) is used to acquire approximation with worst-case error metric as a constraint. A novel technique is proposed to select nodes for insertion of LUTs is discussed. The method evolved around toggle count and observability of nodes in the circuit. The number of transistors used, and errors is examined for analysis. This analysis will help in evaluating the output of the adder circuit obtained through approximation. This method was implemented using Yosys and evaluated adder circuit. The aim of this paper is to adopt formal methods such as satisfiability solvers for analysis of approximate adder circuits. When the worst-case absolute error and area are taken into account for 64 bit, 32 bit and 16 bit our solution will provide a superior trade-off.

Keywords

SAT Approximation LUT Adder circuits

Approximate computing

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▼ Chapter

EUR 29.95

Price includes VAT (India)

- DOI: 10.1007/978-3-031-21514-8_36
- Chapter length: 15 pages
- Instant PDF download
- Readable on all devices

Acknowledgment

This work is supported by Visvesvaraya Ph.D. Scheme, Meity, Govt. of India. MEITY-PHD-2950.

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About this paper

Cite this paper

Choudhary, P., Bhargava, L., Fujita, M., Singh, V. (2022).
Synthesis of LUT Based Approximating Adder Circuits with
Formal Error Guarantees. In: Shah, A.P., Dasgupta, S., Darji,
A., Tudu, J. (eds) VLSI Design and Test. VDAT 2022.
Communications in Computer and Information Science, vol
1687. Springer, Cham. https://doi.org/10.1007/978-3-031-21514-8_36

[.RIS](#)  [.ENW](#)  [.BIB](#) 

DOI

https://doi.org/10.1007/978-3-031-21514-8_36

Published	Publisher Name	Print ISBN
17 December 2022	Springer, Cham	978-3-031-21513- 1

Online ISBN	eBook Packages
978-3-031-21514- 8	Computer Science Computer Science (R0)

Not logged in - 49.36.236.180

Malaviya National Institute of Technology Jaipur (3000189115) - INDEST AICTE Consortium Indian Institute of Technology
(3000185589) - INDEST AICTE Consortium C/o Indian Institute of Technology (3000188743)

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