




## International Symposium on VLSI Design and Test

VDAT 2022: **VLSI Design and Test** pp 435–449

[Home](#) > [VLSI Design and Test](#) > Conference paper

# Synthesis of LUT Based Approximating Formal Error

[Pooja Choudhary](#) ,  
[Virendra Singh](#)

**Lava Bhargava**  [View ORCID ID profile](#)

Department of Electronics and Communication Engineering, Malaviya  
National Institute of Technology, Jaipur, 302017, India

[View author publications](#)

Conference paper | [E](#)

**586** Accesses | **1** Citations

You can also search for this author in  
[PubMed](#) | [Google Scholar](#)

Part of the [Communications in Computer Science](#) book series (CCIS, volume 1687)

## Abstract

Approximate computing relaxes accuracy, enhance efficiency, and benefit in terms of area. It is widely popular in emerging applications like mining, search, vision, recognition where inaccuracies are tolerable. This tolerance towards errors is exploited to design circuits. The most crucial stage is to strike the proper balance between error and output quality. A systematic framework is used for