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Effect of TiW blocking layer and temperature annealing on resistive switching parameters of Hafnium oxide based CBRAM device

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Abstract

An approach for enhancing the characteristics of resistive switching in the crystalline Hafnium oxide-based CBRAM (Conductive Bridging Resistive Switching Memory) device is reported in this article. The crystalline Hafnium oxide resistive switching layer and the TiW blocking layer are beneficial for controlling filament growth. Improved resistive parameters, including stability and resistance distribution, were successfully demonstrated in Cu/TiW/annealed-HfO_2/Pt devices compared to Cu/HfO_2/Pt-based devices. Moreover, the proposed bipolar device demonstrates improved memory performance, such as good retention characteristics ($>10^4$ s) and a high ON/OFF resistance ratio.

1. Introduction

RRAM (Resistive random access memory) technology has emerged as one of the most promising and dependable alternatives to FLASH's scalability limitation in recent years [1–9]. Since its low operating voltage, strong retention, big memory window, and excellent scalability, CBRAM has been a significant rival in recent years [9–12]. In a CBRAM device, resistive switching (RS) is employed. It is based on the formation and breakdown of conductive filaments (CF) caused by the oxidation and reduction of metal ions such as Cu+ and Ag+ [13]. However, because of the random nature of CF creation and rupture, the process is challenging to regulate, resulting in a wide range of switching voltages and resistances in CBRAM devices. Some of the previous work is compared for the better understanding of the proposed work as shown in table 1.

In the research, it has been shown that the CBRAM devices based on the HfO_2 RS-layer exhibit outstanding switching characteristics. However, shrinking the memory window is a huge problem to solve [24]. We provide a very efficient and straightforward approach for addressing the issues of endurance and reliability deterioration in traditional CBRAM devices that arise due to the frequent switching cycles they experience. According to the proposed device's architecture, a TiW diffusion blocking layer (DBL) is placed between the Cu top electrode and the polycrystalline-Hafnium oxide RSL. In addition, the Cu/TiW/annealed-HfO_2/Pt crossbar structure has good memory performance, as shown by a more fantastic ON/OFF resistance ratio and good retention properties.

2. Device fabrication and experiment setup

First, a bottom electrode of Pt with a thickness of 50 nm is deposited using the sputtering process. After that, a sputtering process is used to deposit an HfO_2 layer having a thickness of 10 nm. This HfO_2 layer is a dielectric layer. Finally, using the electron beam evaporation technique at room temperature to create the Cu/HfO_2/Pt CBRAM device structure, a copper top electrode (100 nm thickness) is deposited. An additional TiW layer of 2 nm thickness is additionally deposited by the sputtering method for diffusion blocking. The HfO_2 is annealed at 400 °C in a vacuum environment for the enhanced CBRAM device. The proposed device's current-voltage (I–V) characteristics are measured using a Keysight B1500A semiconductor parameter analyser. We applied bias