SPRINGER LINK

Log in

≡ Menu

Q Search

Cart



International Symposium on VLSI Design and Test

VDAT 2022: VLSI Design and Test pp 435–449

<u>Home</u> > <u>VLSI Design and Test</u> > Conference paper

Synthesis of LUT Based

Approximating Adder Circuits with

Formal Error Guarantee

<u>Pooja Choudhary</u> [™], <u>Lava Bhargava</u>, <u>Virendra Singh</u>

Conference paper | First Online: 17 [

586 Accesses | 1 Citations

Part of the <u>Communications in Comp</u> <u>Science</u> book series (CCIS,volume 16)

Masahiro Fujita Diew ORCID ID profile

Design and Education Center, VLSI, University of Tokyo, Bunkyo City, Japan

View author publications

You can also search for this author in PubMed | Google Scholar

Abstract

Approximate computing relaxes accuracy, enhance efficiency, and benefit in terms of area. It is widely popular in emerging applications like mining, search, vision, recognition where inaccuracies are tolerable. This tolerance towards errors is exploited to design circuits. The most crucial stage is to strike the proper balance between error and output quality. A systematic framework is used for