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Modelling and Control of Active-Clamp Forward Converter for Scalable DC-microgrid

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Abstract. *This paper provides circuit analysis of low-side active-clamp forward converter with synchronous rectification which is used as an efficient power supply in scalable DC-microgrid. With the use of active clamp technique and synchronous rectification techniques, the losses of the converter reduce. Small-signal modeling of the converter and voltage-mode control scheme of the converter has been discussed in this work.*

Index Terms— Forward Converter, Active Clamp, Synchronous Rectification, small-signal modeling, voltage mode control

I INTRODUCTION

To provide reliable and uninterrupted power to different low and medium income households around the world, a lot of research is going on in the direction of modular and scalable DC microgrid. The scalable DC microgrid provides reliable power to household appliances. There are basically 3 different types of microgrids such as

a. Central generation with central storage architecture (CGCSA)
b. Central generation with distributed storage architecture (CGDSA)
c. Distributed generation with distributed storage architecture (DGDSA)

Among these three type of microgrids, CGDSA are preferred due to their higher flexibility and efficiency.
Figure 1 illustrates the schematic diagram of PV-based scalable microgrid. The PV-panel is integrated to HV DC bus using boost converter (380V-400V). The HV DC bus is converted to LV DC-bus (48V) using isolated buck converter. Different DC and AC loads of various voltage levels are connected to the LV-DC bus. DC-load of 12V and 5V are interfaced to LV DC-bus using isolated buck converter. The inverter is used for AC loads. The HV DC bus is further connected to inverter and the inverter is connected to transformer and passive filters which is then interfaced to the electricity grid. The control aspects of HV DC bus and grid has been provided in the schematic diagram.

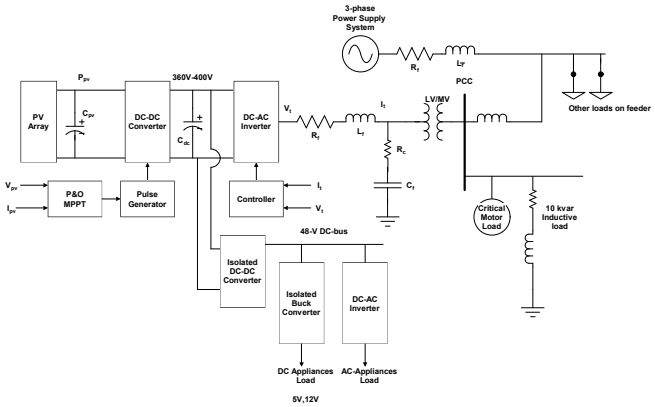

Figure 1 : SCHEMATIC DIAGRAM OF SCALABLE DC MICROGRID

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There are different DC-DC converter topologies used for interfacing the DC loads of household appliances to the LV bus. Forward DC-DC converter is an isolated version of buck converter which are widely used in telecommunication, space application, scalable DC microgrid or low voltage DC microgrid, and computer applications because of its simple circuit, low ripple voltage and high current carrying capability. To reduce the switching loss in the conventional forward converter, active and passive clamping circuit are used.

Performance analysis of input parallel output series (IPOS) modular forward converter has been discussed in [1]. Peak current control of forward converter has been discussed in [2] whereas a comparative analysis of magnetic design for forward converter has been discussed in [3]. Control of Multiple output forward converter has been discussed in [4]. In an isolated converter, there are number of ways by which the transformer can be reset. One of the widely used technique to reset the transformer is active clamp method where auxiliary switch and capacitor are used for the purpose [5-7]. The additional capacitor provides requisite energy to the different cycle and keeps the voltage ripple to minimum. Effect of optocoupler feedback dynamics on peak current mode controlled active-clamp forward converter (ACFC) hasbeen discussed in [8]. In [9], modeling of buck converter is investigated. In [10-11], different high gain DC-DC converter topologies are reviewed and compared. In [12], the authors provide detailed modelling and analysis of high-side ACFC whereas in [13] authors have provided detailed circuit analysis and controller design for low-side ACFC.

This paper provides the circuit operation of classical forward converter, low-side ACFC with synchronous rectification (SR). Circuit analysis, small signal modelling and controller design for the converter has been discussed in this work

II FORWARD CONVERTER: CIRCUIT ANALYSIS

The circuit diagram of classical single-switch forward converter is illustrated in Figure 2. It comprises of a primary winding and a secondary winding with uncontrolled as well as controlled switches. S is the controlled switch (MOSFET) whereas D1, D2 and D3 are the uncontrolled switch (diode).

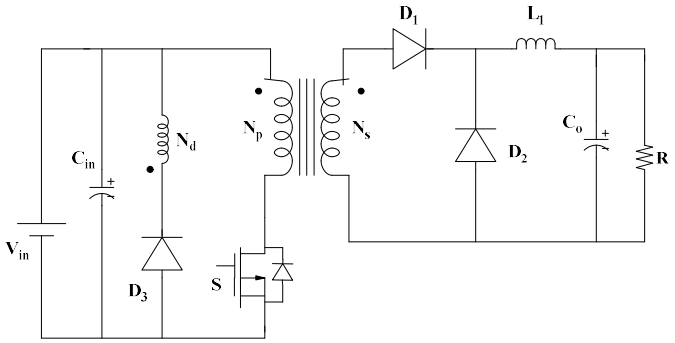


Figure 2 CIRCUIT DIAGRAM OF PRACTICAL FORWARD CONVERTER

The secondary side inductance is calculated as $L_s = \dfrac{L_p}{\left(\dfrac{n_p}{n_s}\right)^2}$ (1)

The current ripple is calculated as $I_r = \dfrac{1}{L_1}\left(V_{in}\left(\dfrac{n_s}{n_p}\right) - V_f - V_o\right)t_1$ (2)

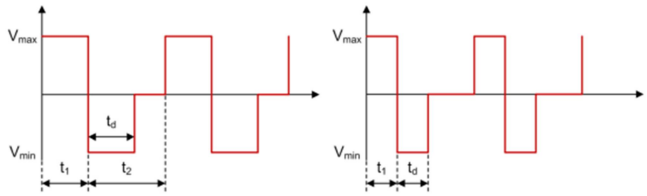


FIGURE 3(a) VOLTAGE WAVEFORMS OF FORWARD CONVERTER DURING CCM AND DCM

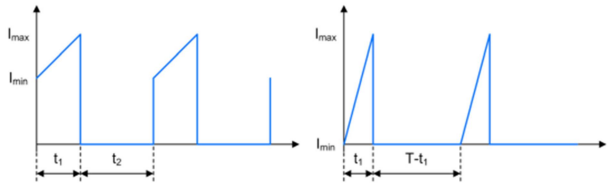


FIGURE 3(b) CURRENT WAVEFORMS OF FORWARD CONVERTER DURING CCM AND DCM

Figure 3(a) & 3(b) illustrates the working principle of forward converter and waveforms of voltage and current of forward converter during continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

III LOW SIDE ACTIVE CLAMP FORWARD CONVERTER

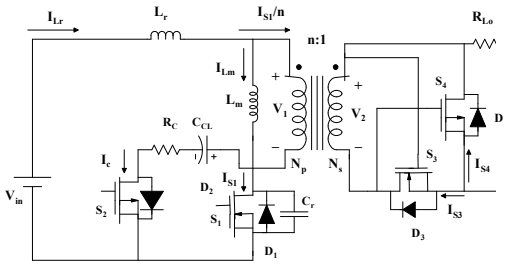


FIGURE 4 CIRCUIT DIAGRAM OF LOW SIDE ACTIVE CLAMP FORWARD CONVERTER

Figure 4 illustrates a low-side ACFC with SR where a p-channel MOSFET is used as an auxiliary switch in both primary and secondary side. The clamp circuit resets the transformer magnetizing inductance because of the clamp circuit, the forward converter achieves zero voltage switching capability and the converter is capable to operate at duty cycle more than 0.5. The following assumptions are considered for the converter

a. Magnetizing inductance is larger than resonant inductance
b. Clamp capacitor larger than resonant capacitor

The minimum value of inductor is represented as

$$L = \left(\frac{V_o}{\Delta I_L I_o f_{osc\_\min}} \right) \left(1 - d_{\min}\right) \tag{3}$$

The minimum value of clamping capacitor is represented as

$$C_c = 10 \left(\frac{1}{L_m \left(2\pi f_{osc\_\min}\right)^2} \right) \left(1 - d_{\min}\right)^2 \tag{4}$$

In low side clamp, $$V_{DS} = \frac{V_{in}}{1-d},\ V_{reset} = \frac{V_{in}d}{1-d} \tag{5}$$

IV SMALL SIGNAL MODELLING

The small signal model of low-side ACFC with SR has been computed in this section. Four different state variables are considered and a 4th order model has been created for the converter. The state variables are (a) magnetizing current, (b) voltage across clamp capacitor, (c) output filter inductor current and (d) output filter capacitor voltage

In ON state, the state space of the converter can be represented as

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & \frac{-1}{RC_o} \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{6}$$

$$V_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} \tag{7}$$

In OFF state, the state space of the converter can be represented as

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_m} & 0 & 0 \\ \frac{1}{C_{CL}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_o} \\ 0 & 0 & \frac{1}{C} & \frac{-1}{RC_o} \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{8}$$

$$V_o = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} \tag{9}$$

State-space average model of converter has been represented as

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-D'}{L_m} & 0 & 0 \\ \frac{D'}{C_{CL}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & \frac{-1}{RC_o} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_m} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{10}$$

Converter with parasitics

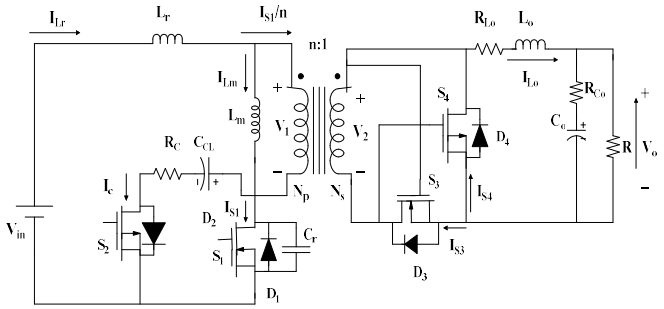


FIGURE 5 CIRCUIT DIAGRAM OF LOW-SIDE ACFC WITH SR WITH PARASITICS

Figure 5 represents the different parasitics involved in low side ACFC with SR with parasitics. The state-space model of low side ACFC with SR with parasitics has been discussed below. In this model, the input voltage output current are considereed as control variable. When the switch is ON, the state space model can be represented as

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{Lo}+R_{co}}{L_o} & -\frac{1}{L_o} \\ 0 & 0 & \frac{1}{C_o}-\frac{R_{co}}{R_oC_o} & -\frac{1}{C_oR} \end{bmatrix} \begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix}$$

$$+\begin{bmatrix} \frac{1}{L_m} & 0 \\ 0 & 0 \\ \frac{1}{L_oN_2} & \frac{R_{co}}{L_o} \\ 0 & \frac{R_{co}}{RC_o} \end{bmatrix} \begin{bmatrix} V_{in} \\ i_o \end{bmatrix} \tag{11}$$

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\dfrac{R_{Lo}+R_{co}}{L_o} & -\dfrac{1}{L_o} \\ 0 & 0 & \dfrac{1}{C_o}-\dfrac{R_{co}}{R_oC_o} & -\dfrac{1}{C_oR} \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_m} & 0 \\ 0 & 0 \\ \dfrac{1}{L_oN_2} & \dfrac{R_{co}}{L_o} \\ 0 & \dfrac{R_{co}}{RC_o} \end{bmatrix}\begin{bmatrix} V_{in} \\ i_o \end{bmatrix} \tag{12}$$

When the switch is OFF, then the state space model of the converter can be represented as

$$\frac{d}{dt}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_c}{L_m} & -\dfrac{1}{L_m} & 0 & 0 \\ \dfrac{1}{C_{CL}} & 0 & 0 & 0 \\ 0 & \dfrac{1}{L_oN_2} & -\dfrac{R_{Lo}+R_{co}}{L_o} & -\dfrac{1}{L_o} \\ 0 & 0 & \dfrac{1}{C_o}-\dfrac{R_{co}}{R_oC_o} & -\dfrac{1}{C_oR} \end{bmatrix}\begin{bmatrix} i_m \\ v_{cc} \\ i_{Lo} \\ v_{co} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_m} & \dfrac{R_c}{N_2L_m} \\ 0 & -\dfrac{1}{C_{CL}N_2} \\ -\dfrac{1}{L_oN_2} & \dfrac{R_{co}}{L_o} \\ 0 & \dfrac{R_{co}}{RC_o} \end{bmatrix}\begin{bmatrix} V_{in} \\ i_o \end{bmatrix} \tag{13}$$

Resulting transfer function of voltage to duty cycle transfer function of low-side ACFC with SR and parasitics has been provided here. The transfer function can be represented as

$$G_{vd}(s) = K\frac{\left(1+\dfrac{s}{\omega_{esr}}\right)\left(1+\dfrac{s}{Q_{n1}\omega_{n1}}+\dfrac{s^2}{\omega_{n1}^2}\right)}{\left(1+\dfrac{s}{Q_{d1}\omega_{d1}}+\dfrac{s^2}{\omega_{d1}^2}\right)\left(1+\dfrac{s}{Q_{d2}\omega_{d2}}+\dfrac{s^2}{\omega_{d2}^2}\right)} \tag{14}$$

$$\text{Where } K = \frac{2V_{in}R}{N\left(R_{Lo}+R\right)}, \tag{15}$$

$$Q_{n1} = \sqrt{\frac{2\left(d-1\right)L_m}{C_{CL}R_c^2\left(2d-1\right)}} \tag{16}$$

$$\omega_{n1} = \sqrt{\frac{2}{L_m C_{CL}\dfrac{\left(2d-1\right)}{\left(d-1\right)^3}}} \quad \omega_{d1} = \sqrt{\frac{R_{Lo}+R}{L_o C_o R}} \tag{17}$$

$$Q_{d1} = \frac{R_{Lo}+R}{\left(C_o R\left(R_{Lo}+R_{co}\right)+L_o\right)\omega_{d1}} \quad \omega_{d2} = \sqrt{\frac{\left(1-D\right)^2}{L_m C_{CL}}} \tag{18}$$

$$Q_{d2} = \frac{1}{R_c}\sqrt{\frac{L_m}{C_{CL}}} \text{ and } \omega_{est} = \frac{1}{C_o R_{co}} \tag{19}$$

V FEEDBACK CONTROL SCHEME

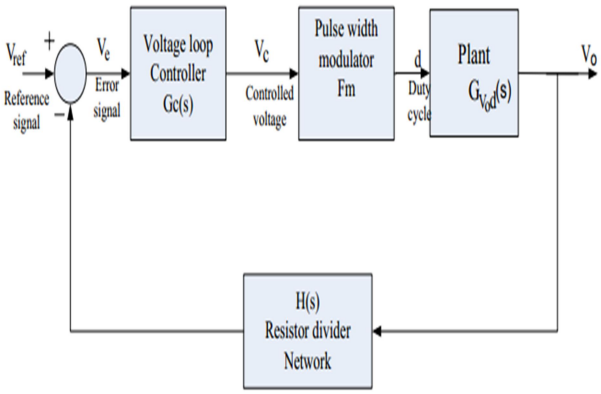


FIGURE 6 FEEDBACK CONTROL SCHEME FOR POWER CONVERTER

Figure 6 illustrates the feedback control scheme for power converter where voltage mode control scheme is used. The PWM modulator is used to provide gate pulse to the converter. The converter dynamics is obtained from the small signal model. Resistor divider network is used for voltage sensing. The generalized form of controller for power converter can be represented as

$$G_c\left(s\right) = K\frac{\left(1+\dfrac{s}{\omega_{z1}}\right)\left(1+\dfrac{s}{\omega_{z2}}\right)}{s\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{s}{\omega_{p2}}\right)} \tag{20}$$

VI SIMULATION ANALYSIS

The specification of a low-side ACFC with SR are as follows

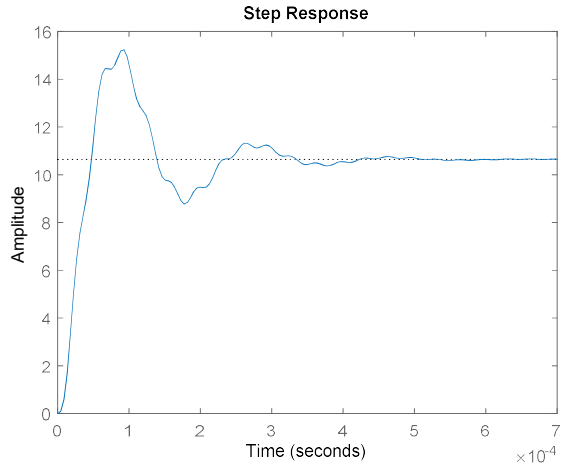
a. Nominal voltage = 48 VDC
b. Output voltage = 5 V DC
c. Output current = 20 A
d. Output current ripple = 30 mA (p-p)
e. Output voltage ripple = 10%
f. Switching frequency = 100 kHz

The converter parameters are Lo = 3.5 µH, Lm = 38 µH, Co = 240 µF and C_{CL} = 240 nF. Transformation ratio is 4.5
The voltage to duty ratio of low side ACFC with SR can be represented as

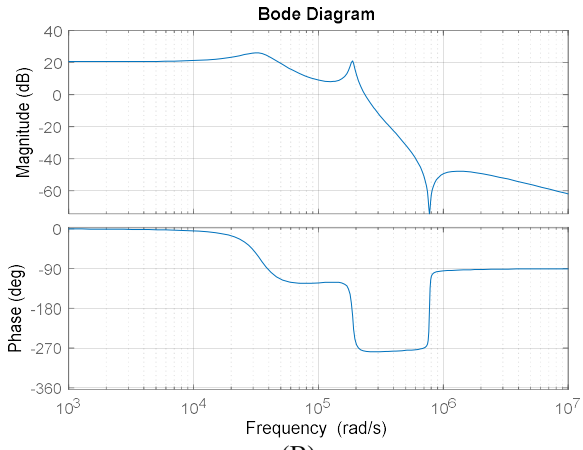
$$G_{vd}(s)=\frac{8067.2269\left(s+9.259\times10^{4}\right)\left(s^{2}+1.328\times10^{4}s+5.997\times10^{11}\right)}{\left(s^{2}+2.079\times10^{4}s+1.193\times10^{9}\right)\left(s^{2}+1.328\times10^{4}s+3.528\times10^{10}\right)}$$

The controller designed for the converter can be represented as

$$G_{c}(s)=9003\frac{(s+350)(s+26666)}{s(s+500)(s+133333)}$$

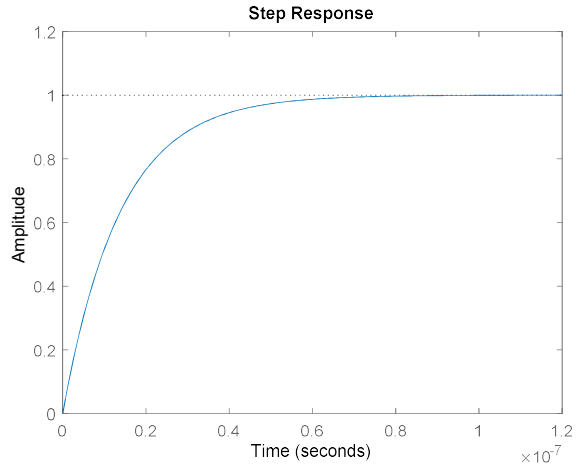


(A)

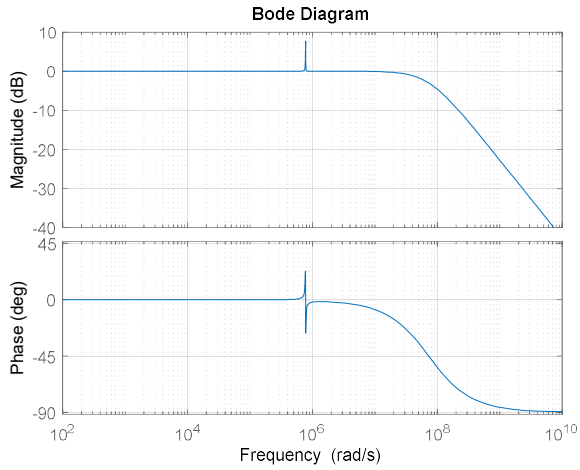


(B)

FIGURE 7. RESPONSE OF UNCOMPENSATED CONVERTER (A) STEP RESPONSE, (B) BODE DIAGRAM



(A)



(B)

FIGURE 8. RESPONSE OF COMPENSATED CONVERTER (A) STEP RESPONSE AND (B) FREQUENCY RESPONSE

Figure 7 and 8 provides the uncompensated and compensated response of the low-side ACFC with SR along with parasitics.

VII CONCLUSION

This paper provides a detailed circuit analysis of low-side ACFC with SR used in scalable microgrid where this converter is used to provide power to low voltage house hold applications. Small signal modelling and controller design of the converter has been discussed in this paper. Simulation results and experimental analysis have been provided for the converters.

VIII REFERENCES

Linns T Alex, Subhransu Sekhar Dash, R Sridhar, "Performance analysis of modular forward converter in input parallel output series (IPOS) architecture using PI and fuzzy logic controller," International Journal of fuzzy system, vol. 21, no. 5, 2019, pp.1524-1532.

Terukazu Sato, Tadao Nakano, "Parallel operation of peak current controlled forward-type DC-DC converters," Electronics and Communications in Japan, part 2, vol. 71, no. 2, 1988, pp. 1231-1238

H E Tacca, “Flyback vs. forward converter topology comparison based upon magnetic design,” Electronica De Potencia – Revista de la Sobraep, vol. 5, no. 1, 2000, pp. 16-27

Youhao Xi, Praveen K Jain, “A forward converter topology with independently and precisely regulated multiple outputs,” IEEE Transactions on Power Electronics, vol. 18, no. 2, Mar 2003, pp. 648-658

Jung, Jee-Hoon, and Shehab Ahmed. "Low standby power consumption and high cross regulation of active clamp flyback converter with SSPR", IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010

Jung, J.-H., and S. Ahmed. "Flyback converter with novel active clamp control and secondary side post regulator for low standby power consumption under high-efficiency operation", IET Power Electronics, 2011, (Volume 4, Issue 9, Page(s) 1058 – 1067).

B-R Lin, Huann-Keng Chiang; Chien-En Huang; David Wang. "Analysis, Design and Implementation of an Active Clamp Forward Converter with Synchronous Rectifier", TENCON 2005 - 2005 IEEE Region 10 Conference, 11/2005

Maturi Krishnaraj, Susovan Samanta, “Effect of optocoupler feedback dynamics on peak current mode controlled active clamp forward converter,” Proc. 2018 IEEMA Engineer Infinite Conference (eTechNxT), 2018, pp. 1-6

Debanjana Bhattacharyya, Subhransu Padhee, Kishor Chandra Pati, “Modelling of DC-DC Converter using Exact-Feedback Linearization Method: A Discussion,” IETE Journal of Research, vol. 65, no. 6, 2019, pp. 843–854

Subhransu Padhee, Umesh Chandra Pati and Kamalakanta Mahapatra, “Overview of High-Step-Up DC-DC Converters for Renewable Energy Sources,” IETE Technical Review, vol. 35, no. 1, 2018, pp. 99–115.

Subhransu Padhee, Umesh Chandra Pati and Kamalakanta Mahapatra, “Comparative analysis of DC-DC converter topologies for fuel cell based application,” in Proc. IEEE Int. Conf. Power Electronics, Intelligent Control and Energy Systems, New Delhi, India, Jul. 2016, pp. 1–6

Krishna Maturi, Susovan Samanta, “Modeling of high-side active clamp forward converter with resistive parasitics,” COMPEL – The international Journal for Computation and Mathematics in Electrical and Electronic Engineering, vol. 39, no. 2, 2020, pp. 413-430.

Shin-Ju Chen and Huang-Chang Chang, “Analysis and implementation of low-side active clamp forward converters with synchronous rectification,” 33rd Annual conf. IECON, 2007