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Approximate Adder Circuits: A Comparative Analysis and Evaluation

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Abstract

Approximate Computing has emerged as a and less complex designs for circuits. Appro that achieves power and area efficiency by i circuit's output behavior. In arithmetic circ become essential to understand the approx performance and efficiency. This paper aim

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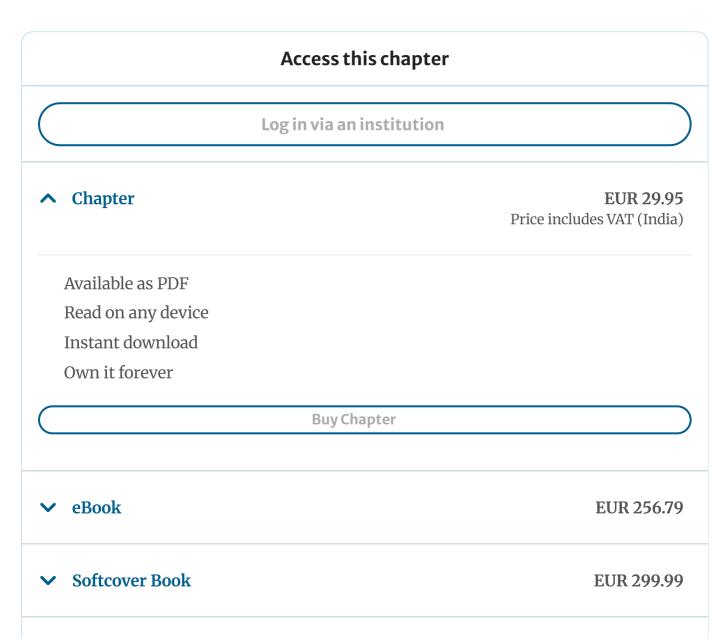
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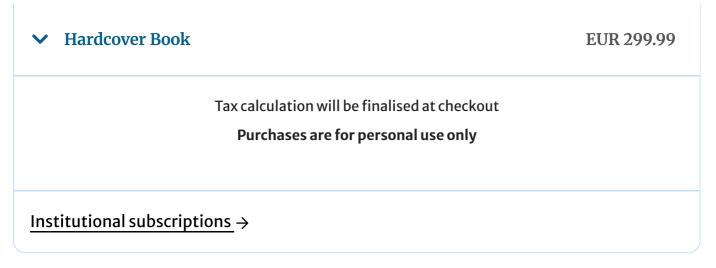
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approximate adders and comparatively asseen approximate adders and comparatively asseen a power. Arithmetic circuits are implemented and synthesized using HDLs and design compiler and error characterization is done by using MATLAB. In this paper power, speed and area are compared with respect to error distance, normalized mean error distance and mean relative error distance. The comparative result conveys that equal segmentation adder has low accuracy but it is a hardware efficient design. After evaluation analysis conveys that equally accurate adders are error-tolerant adder type II, Speculative carry select adder and the accuracy configurable approximate adder. In this most power consuming adder is almost the correct adder. Among all adders, the slowest and extremely efficient adder is the lower part OR adder.

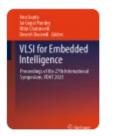
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References

 Han J, Orshansky M (2013) Approximate computing: an emerging paradigm for energy-efficient design. In: 2013 18th IEEE European test symposium (ETS), Avignon, France. IEEE, pp 1–6

Google Scholar

2. Hegde R, Shanbhag NR (2001) Soft digital signal processing. IEEE Trans Very Large Scale Integration VLSI Syst IEEE 9(6):813–823

3. Liu Y, Zhang T, Parhi KK (2009) Computation error analysis in digital signal processing systems with overscaled supply voltage. IEEE Trans Very Large Scale Integr VLSI Syst IEEE 18(4):517–526

Article Google Scholar

4. Mohapatra D, Chippa VK, Raghunathan A, Roy K (2011) Design of voltage-scalable meta-functions for approximate computing. In: 2011 Design, automation & test in Europe, Grenoble, France. IEEE, pp 1–6

Google Scholar

5. Koren I (2002) Computer arithmetic algorithms, 2nd edn. A K Peters

Google Scholar

6. Parhami B (2010) Computer arithmetic, vol 20. Oxford University Press, New York, NY

Google Scholar

7. Lu SL (2004) Speeding up processing with approximation circuits. Comput IEEE 37(3):67–73

Article Google Scholar

8. Rabinowitz P (1961) Multiple-precision division. Commun ACM 4(2):98

Article Google Scholar

9. Goldschmidt RE (1964) Applications of division by convergence. Doctoral dissertation, Massachusetts Institute of Technology

10. Mitchell JN (1962) Computer multiplication and division using binary logarithms. IRE Trans Electron Comput IEEE 4(11):512–517

Article MathSciNet Google Scholar

11. Lim YC (1992) Single-precision multiplier with reduced circuit complexity for signal processing applications. IEEE Trans Comput IEEE 41(10):1333–1336

Article Google Scholar

12. Schulte MJ, Swartzlander EE (1993) Truncated multiplication with correction constant [for DSP]. In: Proceedings of IEEE workshop on VLSI Signal Processing, Veldhoven, Netherlands. IEEE, pp 388–396

Google Scholar

13. Burks AW, Goldstine HH, Neumann JV (1982) Preliminary discussion of the logical design of an electronic computing instrument. In: The origins of digital computers, Berlin, Heidelberg. Springer, pp 399–413

Google Scholar

14. Verma AK, Brisk P, Ienne P (2008) Variable latency speculative addition: a new paradigm for arithmetic circuit design. In: Proceedings of the conference on design, automation and test in Europe, Munich, Germany. ACM, pp 1250–1255

Google Scholar

15. Zhu N, Goh WL, Wang G, Yeo KS (2010) Enhanced low-power high-speed adder for error-tolerant application. In: 2010 International SoC design conference, Incheon, Korea. IEEE, pp 323–327

16. Mahdiani HR, Ahmadi A, Fakhraie SM, Lucas C (2009) Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications. IEEE Trans Circuits Syst I Regul Pap 57(4):850–862

Article MathSciNet Google Scholar

17. Venkataramani S, Sabne A, Kozhikkottu V, Roy K, Raghunathan A (2012) SALSA: systematic logic synthesis of approximate circuits. In: DAC Design automation conference, San Francisco, CA, USA. IEEE, pp 796–801

Google Scholar

18. Vasicek Z, Sekanina L (2014) Evolutionary approach to approximate digital circuits design. IEEE Trans Evol Comput IEEE 19(3):432–444

Article Google Scholar

19. Mrazek V, Sarwar SS, Sekanina L, Vasicek Z, Roy K (2016) Design of power-efficient approximate multipliers for approximate artificial neural networks. In: 2016 IEEE/ACM International conference on computer-aided design (ICCAD), Austin, TX,USA. ACM, pp 1–7

Google Scholar

20. Kahng AB, Kang S (2012) Accuracy-configurable adder for approximate arithmetic designs. In: Proceedings of the 49th annual design automation conference, San Francisco, California. ACM, pp 820–825

Google Scholar

21. Zhu N, Goh WL, Yeo KS (2011) Ultra low-power high-speed flexible probabilistic adder for error-tolerant applications. In: 2011 International SoC design conference,

Jeju, Korea. IEEE, pp 393–396

Google Scholar

22. Miao J, He K, Gerstlauer A, Orshansky M (2012) Modeling and synthesis of qualityenergy optimal approximate adders. In: Proceedings of the International conference on computer-aided design, San Jose, California, pp 728–735

Google Scholar

23. Yang X, Xing Y, Qiao F, Wei Q, Yang H (2016) Approximate adder with hybrid prediction and error compensation technique. In: 2016 IEEE Computer society annual symposium on VLSI (ISVLSI), Pittsburg, PA, USA. IEEE, pp 373–378

Google Scholar

24. Camus V, Schlachter J, Enz C (2016) A low-power carry cut-back approximate adder with fixed-point implementation and floating-point precision. In: 2016 53nd ACM/EDAC/IEEE Design automation conference (DAC), Austin, TX, USA. IEEE, pp 1–6

Google Scholar

25. Ebrahimi-Azandaryani F, Akbari O, Kamal M, Afzali-Kusha A, Pedram M (2019) Block-based carry speculative approximate adder for energy-efficient applications. IEEE Trans Circuits Syst II Express Briefs IEEE 67(1):137–141

Google Scholar

26. Du K, Varman P, Mohanram K (2012) High performance reliable variable latency carry select addition. In: 2012 Design, automation & test in europe conference & exhibition (DATE), Dresden, Germany. IEEE, pp 1257–1262

Google Scholar

27. Kim Y, Zhang Y, Li P (2013) An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems. In: 2013 IEEE/ACM International conference on computer-aided design (ICCAD), San Jose, CA, USA. IEEE, pp 130–137

Google Scholar

28. Ye R, Wang T, Yuan F, Kumar R, Xu Q (2013) On reconfiguration-oriented approximate adder design and its application. In: 2013 IEEE/ACM International conference on computer-aided design (ICCAD), San Jose, CA, USA. IEEE, pp 48–54

Google Scholar

29. Lin C, Yang YM, Lin CC (2014) High-performance low-power carry speculative addition with variable latency. IEEE Trans Very Large Scale Integr VLSI Syst IEEE 23(9):1591–1603

Article Google Scholar

30. Li L, Zhou H (2014) On error modeling and analysis of approximate adders. In: 2014 IEEE/ACM International conference on computer-aided design (ICCAD), San Jose, CA, USA. IEEE, pp 511–518

Google Scholar

31. Hu J, Qian W (2015) A new approximate adder with low relative error and correct sign calculation. In: 2015 Design, automation & test in Europe conference & exhibition (DATE),Grenoble, France. IEEE, pp 1449–1454

Google Scholar

32. Gupta V, Mohapatra D, Raghunathan A, Roy K (2012) Low-power digital signal processing using approximate adders. IEEE Trans Comput Aided Des Integr Circuits Syst, IEEE 32(1):124–137

33. Yang Z, Jain A, Liang J, Han J, Lombardi F (2013) Approximate XOR/XNOR-based adders for inexact computing. In: 2013 13th IEEE International conference on nanotechnology (IEEE-NANO 2013), Beijing, China. IEEE, pp 690–693

Google Scholar

34. Almurib HAF, Kumar TN, Lombardi F (2016) Inexact designs for approximate low power addition by cell replacement. In: 2016 Design, automation & test in Europe conference & exhibition (DATE), Dresden, Germany. IEEE, pp 660–665

Google Scholar

35. Pashaeifar M, Kamal M, Afzali-Kusha A, Pedram M (2018) Approximate reverse carry propagate adder for energy-efficient DSP applications. IEEE Trans Very Large Scale Integr VLSI Syst, IEEE 26(11):2530–2541

Article Google Scholar

36. Angizi S, Jiang H, DeMara RF, Han J, Fan D (2018) Majority-based spin-CMOS primitives for approximate computing. IEEE Trans Nanotechnol IEEE 17(4):795–806

Google Scholar

37. Mrazek V, Hrbacek R, Vasicek Z, Sekanina L (2017) EvoApprox8b: library of approximate adders and multipliers for circuit design and benchmarking of approximation methods. In: Design, automation & test in Europe conference & exhibition (DATE), Lausanne, Switzerland. IEEE, pp 258–261

Google Scholar

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38. Liu C, Han J, Lombardi F (2014) An analytical framework for evaluating the error characteristics of approximate adders. IEEE Trans Comput IEEE 64(5):1268–1281

Article MathSciNet Google Scholar

39. Jiang H, Angizi S, Fan D, Han J, Liu L (2021) Non-volatile approximate arithmetic circuits using scalable hybrid spin-CMOS majority gates. IEEE Trans Circuits Syst I Regul Pap IEEE 68(3):1217–1230

Article Google Scholar

40. Qureshi A, Hasan O (2018) Formal probabilistic analysis of low latency approximate adders. In: IEEE Transactions on computer-aided design of integrated circuits and systems, vol 38, no 1. IEEE, pp 177–189

Google Scholar

 Hanif MA, Hafiz R, Hasan O, Shafique M (2020) PEMACx: a probabilistic error analysis methodology for adders with cascaded approximate units. In: 2020 57th ACM/IEEE Design automation conference (DAC), San Francisco, CA, USA. IEEE, pp 1–6

Google Scholar

42. Jiang H, Liu C, Liu L, Lombardi F, Han J (2017) A review, classification, and comparative evaluation of approximate arithmetic circuits. ACM J Emerg Technol Comput Syst (JETC) ACM 13(4):1–34

Google Scholar

43. Jiang H, Liu L, Lombardi F, Han J (2019) Approximate arithmetic circuits: design and evaluation. In: Approximate circuits. Springer, Cham, pp 67–98

Google Scholar

44. Reda, S, Shafique M (2019). Error analysis and optimization in approximate arithmetic circuits. In: Approximate circuits. Springer, Cham

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