Scheme of

POSTGRADUATE DEGREE COURSE

M.Tech. I to IV Semester

VLSI Design

(Effective from academic session: 2020-21)

Rajasthan Technical University, Kota

Akelgarh, Rawatbhata Road, Kota-324010

RAJASTHAN TECHNICAL UNIVERSITY

M.Tech. (VLSI Design)

Teaching & Examination Scheme (Full Time) w.e.f. 2020-21

Semester I

Sr. No.	Course Type	Course code	Course Name	Teaching Scheme			Marks			Cr
				L	T	P	I	E	T	
1.	PCC	1MVL1-01	Microelectronics	3	0	0	30	70	100	3
2.	PCC	1MVL1-02	Digital system Design	3	0	0	30	70	100	3
3.	PCC	1MVL1-03	Analog VLSI Design	3	0	0	30	70	100	3
4.	PEC	1MVL2-11	Nanoelectronics	3	0	0	30	70	100	3
		1MVL2-12	Low Power VLSI Design							
		1MVL2-13	MEMS							
5.	PCC	1MVL1-06	VLSI Circuit Design Lab	0	0	4	60	40	100	2
6.	PCC	1MVL1-07	Microelectrons Devices & MEMS Design Lab	0	0	4	60	40	100	2
7.	MCC	1MCC4-21	Research Methodology and IPR	2	0	0	30	70	100	2
8.	SODECA	1MVL5-00	Social Outreach discipline & Extra Curriculum Activities					0	100	2
			Total	**14**			**270**	**430**	**800**	**20**

Semester II

Sr. No.	Course Type	Course code	Course Name	Teaching Scheme L	T	P	Marks I	E	T	Cr
1.	PCC	2MVL1-01	Functional Verification using Hardware Verification Languages	3	0	0	30	70	100	3
2.	PCC	2MVL1-02	HDL & FPGA	3	0	0	30	70	100	3
3.	PEC	2MVL2-11	VLSI DSP Architectures	3	0	0	30	70	100	3
		2MVL2-12	Algorithms for VLSI Design Automation							
		2MVL2-13	SOC design							
4.	PEC	2MVL2-14	Mixed Signal ICs	3	0	0	30	70	100	3
		2MVL2-15	ASIC design							
		2MVL2-16	Micro & Nano Fabrication Technology And Processes							
	MCC	2MCC3-XX	Audit course–I	2	0	0				
5.	PCC	2MVL1-06	FPGA Design Lab	0	0	4	60	40	100	2
6.	PCC	2MVL1-07	Advanced VLSI Design Lab	0	0	4	60	40	100	2
7.	REW	2MVL4-50	Mini Project with seminar	2	0	4	60	40	100	2
9.	SODECA	2MVL5-00	Social Outreach discipline & Extra Curriculum Activities					0	100	2
			Total				**300**	**400**	**800**	**20**

Semester III

SN	Course Type	Course code	Course Name	Teaching Scheme L	T	P	Marks I	E	T	Credit
1.	PEC	3MVL2-11	Nanoscale Devices: Modeling& Circuits	3	0	0	30	70	100	3
		3MVL2-12	RF VLSI Circuits							
		3MVL2-13	Testing of VLSI Circuits							
2.	MCC	3MCC3-XX	Audit course-II	2	0	0				0
3.	MCC	3MCC3-XX	Open Elective	3	0	0	30	70	100	3
4.	REW	3MVL4-60	Dissertation phase I: Industrial Project	0	0	20	240	160	400	10
			Total				**300**	**300**	**600**	**16**

Semester IV

SN	Course Type	Course code	Course Name	Teaching Scheme L	T	P	Marks I	E	T	Credit
1.	REW	4MVL4-70	Dissertation phase II	0	0	32	360	240	600	16
			Total				**360**	**240**	**600**	**16**

RAJASTHAN TECHNICAL UNIVERSITY
SYLLABUS: M.Tech. (VLSI Design)

1MVL1-01: Microelectronics

Syllabus:

CONTENTS	CONTACT HOURS
Introduction to semiconductor physics: Review of quantum mechanics, electrons in periodic lattices, E-k diagrams, Quasi-particles in semiconductors, electrons, holes and phonons. Boltzmann transport equation and solution in the presence of low electric and magnetic fields mobility and diffusivity; carrier statistics; continuity equation, poisson's equation and their solution; high field effects: velocity saturation, hot carriers, avalanche breakdown, punch through and kirk effects.	**12**
Semiconductor junctions: Schottky, homo and hetero-junction band diagrams and I-V characteristics, small signal switching models; two terminal and surface states devices based on semiconductor junctions.	**8**
Bipolar transistor working, its charge control, and gummel poon model, structure of graded base, graded emitter transistor, hetro-junction transistor.	**8**
MOS structures: Semiconductor surfaces; the ideal and non-ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; characterization of MOS capacitors: HF and LF CVs, avalanche injection; high field effects and breakdown. Long & short channel effects.	**12**
Total	**40**

Reference books:

1. Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, US, Third Edition, 2011.
2. J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, US, 2017.
3. Streetman and Banerjee, Solid State Electronic Devices, Prentice-Hall
4. Wayne Wolf, “Modern VLSI Design”, PearsonPublication.

1MVL1-02: Digital System Design

Syllabus:

CONTENTS	CONTACT HOURS
Review of CMOS Digital (logic gates, Combinational and sequential) Circuit Design, Schematic and layout design.	**4**
Synchronous Sequential Logic Circuit Design: Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Circuit design of latches and flip-flops. Synchronous sequential design of Moore, Mealy Machines, Synchronous Counter Design, Hazards, Duality of sequential circuits, Different methods of minimization. Static sequencing element methodology. Sequencing static circuits, Sequencing dynamic circuits. Synchronizers.	**10**
Asynchronous Sequential logic design: Introduction, Primitive flow table and reduction, type of delays, Cycles and races, Excitation Map, Hazards, Essential hazards, Analysis of asynchronous sequential circuits. Symmetric and Iterative circuits- Symmetric functions, iterative functions, realization in tree form.	**8**
Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst-case timing analysis. FSM and Hazards.	**5**
Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.	**5**
Reconfigurable Computing: Fine grain and Coarse grain architectures, Configuration architectures Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.	**8**
Total	**40**

Reference books:

1. N.H.E.Weste, D. Harris, "CMOS VLSI Design (4th edition)", Pearson, 2010.
2. W.Wolf, "FPGA- based System Design", Pearson, 2004.
3. S.Hauck&A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008.
4. F.P. Prosser & D. E. Winkel, "Art of Digital Design", 1987.
5. R.F.Tinde, "Engineering Digital Design", (2nd edition), Academic Press, 2000.
6. C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.
7. M.Gokhale&P.S.Graham, "Reconfigurable computing: accelerating computation with fieldprogrammable gate arrays", Springer, 2005.
8. C.Roth," Fundamentals of Digital Logic Design", Jaico Publishers, 5th edition., 2009.
9. Recent literature in Digital System Design.

1MVL1-03: Analog VLSI Design

Syllabus:

CONTENTS	CONTACT HOURS
Introduction to Analog VLSI: Analog integrated circuit design, Circuit design consideration for MOS challenges in Analog circuit design, recent trends in analog VLSI circuits.	**5**
Analog MOSFET Modelling: MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, temperature effects in MOSFET, Noise in MOSFET.	**4**
Current Source, Sinks and References: MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors and advance current mirror using BJT and MOSFET, Current and Voltage references, bandgap references. CMOS Amplifier: Performances matrices of amplifier circuits, Common source amplifier, Common gate amplifier, Cascode amplifier, Frequency response of amplifiers and stability of amplifier.	**6** **5**
CMOS Differential Amplifier: Differential signalling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load, Differential to single ended conversion.	**5**
CMOS Operational amplifier: Block diagram of Op-amplifier, Ideal characteristics of Op-Amplifier, Design of two stage Op-Amplifier, Compensation of Op-Amplifier, Frequency response of Op-Amplifier, Operational Transconductance Amplifier (OTA).	**6**
CMOS Comparator: Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator, Regenerative comparator, High output current amplifier, High speed comparator.	**4**
Introduction to Current mode processing and Current Conveyor, Current Mode Building Blocks: Current Controlled Conveyor (CCC II), current Differencing transconductance Amplifier (CDTA).	**5**
Total	**40**

Reference books:

1. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publication.
2. R. Jacob Baker, Harry W. Li, and David E. Boyce,“CMOS: Circuit Design , Layout and Simulation”, Prentice Hall of India
3. David A. Johns and Ken Martin, “Analog Integrated circuit Design, John Wiley & Sons. 4. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits” Wiley; 5th edition.

1MVL2-11: Nanoelectronics

Syllabus:

CONTENTS	CONTACT HOURS
Quantum & Statistical Mechanics, Wave particle duality and Schr*o*dinger equation, Free and bound particles, Quasi Low-Dimensional Structures Quantum wells, Wires, Dots, Band structure of low-dimensional systems, Quantum confinement, Density-of-states in 2D, 1D and 0D structures, Heterostructures and bandgap engineering, Modulation doping, Strained layer structures Nanoscale MOSFETs Challenges of the CMOS technologies, High-k dielectrics and Gate stack, Future interconnect. MOSFET as digital switch, Propagation delay, Dynamic and static power dissipation Moore‘s law, Transistor scaling, Constant field scaling theory, Constant Voltage Scaling, Generalized scaling, Short channel effects, Reverse short channel effect, Narrow width effect, Subthreshold conduction leakage, Subthreshold slope, Drain Induced Barrier Lowering, Gate Induced Drain Leakage.	**10**
Design of NanoMOSFET: Halo implants, Retrograde channel profile, Shallow source/drain extensions, Twin well CMOS process flow, Gate Tunneling : Fowler Nordheim and Direct Tunneling, High k gate dielectrics, Metal gate transistor, Transport in Nanoscale MOSFET, Ballistic transport, Channel quantization.	**6**
Designing with FINFETs: Evolution of FinFET, Principle of FinFET, Finfet Technology, FinFET Schematic, Compact Drain-Current equation, Small Signal Model of Si- Based FinFET, FinFET Fabrication Flow, Power dissipation in FinFETs, Leakage power reduction techniques, Power gating, Dual sleep, Dual stack, Sleepy stack, Basic gate design using FinFET‘s, combinational logic, sequential logic, Adders, Multiplier, SRAM cell design	**8**
Designing with CNTFETs: Introduction to CNTs, CNT structure, metallic and semiconductor CNTs, energy bands in CNTs, types of CNTs: Single walled and multiwalled, physical, electrical and thermal properties of CNTs, fabrication of CNTs. CNTFETs, structure and model, small signal model, predictive technology models, N-Channel and P-Channel CNTFETs, model files of CNTFETs, basic gates using CNTFET, VI characteristics of CNTFET based inverter, designing of sub systems using CNTFETs, combinational and sequential circuits using CNTFETs, adders, multipliers and SRAM cell using CNTFETs.	**8**
Molecular Nanoelectronics: Electronic and optoelectronic properties of molecular materials, Devices based on quantum wells, quantum wires/nanotubes and quantum dots – HEMTs, RTDs, CNT MOSFETs, SETs, Terahertz devices, advanced optoelectronic devices. TFTs- OLEDs- OTFTs – logic switches, Spintronics: Spin tunneling devices - Magnetic tunnel junctions- Tunneling spin polarization, -spin diodes - Magnetic tunnel transistor - Memory devices and sensors - ferroelectric random-access memory- MRAMS	**8**
Total	**40**

Reference books:

1. Yuan Taur and Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge
2. Karl Goser, Peter Glosekotter, Jan Dienstuhl, ―Nanoelectronics and Nanosystems‖, Springer (2004)
3. Cyril Prasanna Raj P., Designing with FINFETs and CNTFETs, MSEC E-Publication (2016)
4. SadamichiMaekawa, ―Concepts in Spin Electronics‖, Oxford University Press (2006)
5. V. Mitin, V. Kochelap, M. Stroscio, Introduction to Nanoelectronics, Cambridge University Press (2008)
6. Edward L. Wolf, ―Nanophysics and Nanotechnology: An Introduction to Modern Concepts in Nanoscience‖, Wiley-VCH (2006)
7. Streetman and Banerjee, Solid State Electronic Devices, Prentice-Hall
8. Rainer Waser, ―Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH.

1MVL2-12: Low Power VLSI Design

Syllabus:

Topic	CONTACT HOURS
Introduction to low power VLSI design: Need for low power-CMOS leakage current-static current-Basic principles of low power design-probabilistic power analysis-random logic signal-probability and frequency-power analysis techniques-signal entropy.	**10**
Circuit transistor and gate sizing: pin ordering, network restructuring and reorganization adjustable threshold voltages, logic signal gating, logic encoding. Pre-computation logic. Power reduction in clock networks, CMOS floating node, low power bus, delay balancing SRAM. Switching activity reduction, parallel voltage reduction, operator reduction, adiabatic computation, pass transistor logic Low power circuit design style, Software power estimation - co design.	**12**
Low Power Latches and Flip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.	**6**
Low Voltage Low Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative evaluation.	**6**
Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.	**6**
Total	**40**

Reference books:

1. Gary Yeap "Practical Low Power Digital VLSI Design", 1997
2. J.Rabaey, Digital Integrated circuits, PHI Publication.
3. Kaushik Roy ,Sharat C. Prasad, "Low power CMOS VLSI circuit design", Wiley Inter science Publications". (1987)
4. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation.
5. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
6. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication.
7. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication .
8. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National andInternational Conferences and Symposia.

1MVL2-13: MEMS

Syllabus:

CONTENTS	CONTACT HOURS
Introduction to MEMS: Historical background of Micro Electro Mechanical Systems, Feynman 's vision, Nano Technology and its Applications Multi-disciplinary aspects, Basic Technologies, Applications areas, Scaling Laws in miniaturization, scaling in geometry, electrostatics, electromagnetic, electricity and heat transfer.	**6**
Micro and Smart Devices and Systems: Principles Transduction Principles in MEMS Sensors: Micro sensors-thermal radiation, mechanical and bio-sensors, Actuators: Different actuation mechanisms - silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, silicon micro-mirror arrays, piezo-electric based inkjet print head, electrostatic comb-driver, Smart phone application, Smart buildings	**8**
Materials and Micro manufacturing: Semiconducting Materials., Silicon, Silicon dioxide, Silicon Nitride, Quartz, Poly Silicon, Polymers, Materials for wafer processing, Packaging Materials Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding. Silicon micromachining: surface, bulk, LIGA process, Wafer bonding process.	**8**
Electrical and Electronics aspects: Electrostatics, Coupled Electro mechanics, stability and Pull-in phenomenon, Practical signal conditioning Circuits for Microsystems. Characterization of pressure sensors, RF MEMS. Switches varactors, tuned filters. Micromirror array for control and switching in optical communication, Application circuits based on microcontrollers for pressure sensor, Accelerometer, Modeling using CAD Tools.	**8**
Integration and Packaging of Microelectromechanical Systems: Integration of microelectronics and micro devices at wafer and chip levels. Microelectronic packaging: wire and ball bonding, flip-chip. Microsystem packaging examples, Testing of Micro sensors, Qualification of Mems devices Case Study: Fabrication of MEMS based Gas Sensor.	**10**
Total	**40**

Reference books:

1. G. K. Ananthasuresh, K. J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, ―Micro and Smart Systems‖, Wiley India, 2010.
2. T R Hsu, ―MEMS and Microsystems Design and Manufacturing‖, Tata McGraw Hill, 2nd Edition, 2008.
3. Chang Liu, ―Foundations of MEMS‖, Pearson International Edition, 2006.
4. S. D. Senturia, ―Micro System Design‖, Springer International Edition, 2001.

1MVL1-06: VLSI Circuit Design Lab

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/

Session – I: Digital VLSI Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. I-V Curves of NMOS and PMOS Transistors
3. DC Characteristics of CMOS Inverters (VTC, Noise Margin)
4. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)
5. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits
6. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits

Session-II: Analog VLSI Design Laboratory

1. Modeling of Diodes, MOS transistors, Bipolar Transistors etc. using SPICE.
2. Study of MOS Characteristics and Characterization
3. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)
4. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)
5. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)
6. Design and Simulation of Basic Current Mirror, Cascode Current Mirror
7. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier
8. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier.

1MVL1-07: Microelectronics Device and MEMS Design Lab

Module 1: Microelectronics Device and Process Simulation

This module focuses on the simulation of fabrication processes and the microelectronics devices etc.using TCAD tools.

1. short channel MOSFET
2. solar photo voltaic device.
3. HBT
4. FINFET
5. High K Multi Gate MOSFET

The device simulation involves simulating the electrical characteristics of a process simulated/fabricated electronics device.

Module 2: MEMS Design and simulation

This module focuses on design and simulation aspects of sensors, actuators and sensor systems. The laboratory course provides an overview of numerical and analytical modelling and design of microsystems using leading softwares in the field such as TCAD for MEMS. Following MEMS structures have to design and simulate

1. Cantilever
2. MEMS electrostatic Switch
3. Piezoelectric Pressure sensor
4. Design of RLC (lumped) Component
5. Accelerometer

1MCC4-21: Research Methodology and IPR

Syllabus:

CONTENTS	CONTACT HOURS
Meaning of research problem, sources of research problem, criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem, Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations, Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.	**10**
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.	**8**
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.	**4**
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.	**6**
Total	**28**

Reference books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall, "Industrial Design", McGraw Hill, 1992.
6. Niebel, "Product Design", McGraw Hill, 1974.
7. Asimov, "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
9. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008.

Semester II

2MVL1-01: Functional Verification using Hardware Verification Languages

Syllabus:

CONTENTS	CONTACT HOURS
System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Advanced OOPs & Test bench guidelines, Advanced Interfaces.	**8**
A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modelling with SV, Connecting Test bench & Design, Behavioural& Transaction Level Modelling with SV.	**6**
System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single & Multiple Clock definitions, Implication operators (Overlapping & Non-overlapping), Repeatition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property.	**10**
SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice & Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.	**8**
Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, System Verilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, e Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).	**8**
Total	**40**

Reference books:

1. SystemVerilog for design: a guide to using SystemVerilog for hardware design and modeling By Stuart Sutherland, Simon Davidmann, Peter Flake Edition: illustrated Published by Springer, 2004 ISBN 1402075308, 9781402075308.
2. System Verilog for Verification: A Guide to Learning the Test bench Language Features By Chris Spear Edition: 2, Published by Springer, 2008 ISBN 0387765298, 9780387765297.
3. A Practical guide for System Verilog Assertions By Srikanth Vijayaraghavan&MeyyappanRamanathan Edition: illustrated Published by Springer, 2005 ISBN 0387260498, 9780387260495.
4. The Art of Verification with System Verilog Assertions By Faisal I.Haque, Jonathan Michelson, KhizarA.Khan Published by Verification Central 2006 ISBN-13:978-0-97119941-5
5. System-on-a-Chip Verification: Methodology and Techniques by Prakash Rashinkar, Peter Paterson, Leena Singh and Published by Kluwer Academic Publishers 2004, New York, ISBN-0-306-46995-2.

2MVL1-02: HDL & FPGA

Syllabus:

CONTENTS	CONTACT HOURS
HARDWARE MODELING WITH THE VERILOG HDL: Hardware Encapsulation –The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.	**5**
LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOGHDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.	**8**
BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non- Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.	**7**
SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology- Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic, Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.	**8**
SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User- Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.	**6**

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction by Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.	**6**
Total	**40**

Reference books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, McGraw Hill.
3. M.G.ARNOLD, Verilog Digital – Computer Design", Prentice-Hall (PTR).
4. PERRY, "VHDL", McGraw Hill.
5. P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
6. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub.
7. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, New York.
8. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.
9. Richard FJinder , "Engineering Digital Design, "Academic press.

2MVL2-11: VLSI DSP Architectures

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Syllabus:

CONTENTS	CONTACT HOURS
Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance: Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls.	**9**
Data path and control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls.	**8**
Enhancing performance with pipelining: An overview of pipelining, a pipe lined data path, pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards, using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls.	**8**
Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors.	**7**
Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.	**8**
Total	**40**

Reference books:

1. D.A, Patterson, J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier.
2. A.S. Tannenbaum, Structured Computer Organization, 4th Edition, Prentice-Hall
3. W. Wolf, Modern VLSI Design: Systems on Silicon, 2nd Edition, Pearson Education
4. KeshabParhi, VLSI digital signal processing systems design and implementations, Wiley
5. Avatar Sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson.

2MVL2-12: Algorithms for VLSI Design Automation

Syllabus:

CONTENTS	CONTACT HOURS
VLSI physical design automation and Fabrication VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices. VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.	**10**
Floor planning & pin assignment: Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block& cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement.	**12**
Global Routing and Detailed routing: Problem formulation, classification of global Routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.	**10**
Over the cell routing & via minimization: Two layers over the cell routers, constrained & unconstrained via minimization, Compaction, Problem formulation, classification of compaction algorithms, one dimensional compaction, two dimension-based compaction, hierarchical compaction.	**8**
Total	**40**

Reference books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSI Design",Kluwer Academic Publisher.
3. R. Drechsler, "Evolutionary Algorithm for VLSI CAD", Kluwer Academic Publication.

2MVL2-13: SOC Design

Syllabus:

CONTENTS	CONTACT HOURS
Motivation for SoC Design: Review of Moore's law and CMOS scaling, benefits of system-on chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.	**10**
System On Chip Design Process: A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.	**10**
Embedded Memories –cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence. Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC.Packet switching and wormhole routing.	**8**
MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design.	**6**
Case Study: A Low Power Open Multimedia Application Platform for 3G and 4G Wireless Communication Technology.	**6**
Total	**40**

Reference books:

1. SudeepPasricha and NikilDutt,"On-Chip Communication Architectures: System on ChipInterconnect", Morgan Kaufmann Publishers.
2. Rao R. Tummala, MadhavanSwaminathan, "Introduction to system on package sop-Miniaturization of the Entire Syste", McGraw-Hill Publication.
3. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley StudentEdition.
4. Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System on Chipdesigns", Kluwer Academic Publishers, 2nd edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", Tata McGraw-HillPublication.

2MVL2-14: Mixed - Signal ICs

Syllabus:

CONTENTS	CONTACT HOURS
CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations. Voltage Controlled oscillator (VCO) Phase Locked Loop (PLL), Sampled and Hold Circuits Concepts of Mixed-Signal Design and Performance Measures.	**15**
Introduction and Principle behind ADC's and DAC's: Performance Metrics of ADCs and DACs, Nyquist Rate DACs, ComparatorsCharacterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs.	**15**
Design methodology for mixed signal IC design using gm/Id concept. Design of frequency and Q tunable continuous time filters.	**10**
Total	**40**

Reference books:

1. David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 1997.
2. B. Razavi, "Principles of Data Conversion System Design", Wiley-IEEE Press.
3. CMOS Mixed Signal circuit Design, R. J. Baker, Wiley
4. CMOS Data Conversion for Communications, M.Gustavsson, J. J. Wikner, and N. N. Tan,

2MVL2-15: ASIC Design

Syllabus:

CONTENTS	CONTACT HOURS
Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors.	**10**
ASIC physical design issues, System Partitioning, Floorplanning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs & Applications. Schematic and layout basics, Full Custom Design Flow.	**8**
Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, TimingOptimization, GDS generation. Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM.	**12**
System-On-Chip Design: SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.	**10**
Total	**40**

Reference books:

1. M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson, 2003.
2. SudeepPasricha&NikilDutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsevier, 2008.
3. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.
4. Jan.M.Rabaey et al, “Digital Integrated Circuit Design Perspective”, 2nd Edition, PHI 2003.
5. David A.Hodges, “Analysis and Design of Digital Integrated Circuits”, 3rd Edition, MGH 2004.
6. Hoi-Jun Yoo, KangminLee&Jun Kyong Kim, “Low-Power NoC for High-Performance SoC Design”, CRC Press, 2008.
7. “An Integrated Formal Verification solution DSM sign-off market trends”, www.cadence.com.
8. Recent literature in Design of ASICs.

2MVL2-16: Micro- and Nanofabrication Technology and Process

Syllabus:

CONTENTS	CONTACT HOURS
Introduction and overview of micro and nano fabrication technology. Safety and contamination issues in a cleanroom. Overview of cleanroom hazards. Basic process flow structuring. Wafer type selection and cleaning methods. Additive fabrication processes.	**8**
Material deposition methods: Overview of physical vapour deposition methods (thermal, e-beam, molecular beam evaporation) and chemical vapour deposition methods (PE-CVD, MOCVD, CBE, ALD). Pulsed laser deposition (PLD), pulsed electron deposition (PED).	**9**
Doping: diffusion and ion implant techniques. Optical lithography fundamentals, contact lithography, stepper/canner lithography, holographic lithography, direct-laser writing. Lithography enhancement methods and lithography modelling. Non-optical lithography; E-beam lithography, ion beam patterning, bottom-up patterning techniques.	**8**
Etching process: dry and wet. Wet etch fundamentals, isotropic, directional and anisotropic processes. Dry etching process fundamentals, plasma assisted etch process, Deep Reactive Ion Etching (DRIE), Through Silicon Vias (TSV). Isotropic release etch. Chemical-mechanical polishing (CMP), lapping and polishing.	**9**
Packaging and assembly, protective encapsulating materials and their deposition. Wafer dicing, scribing and cleaving. Mechanical scribing and laser scribing, Wafer bonding, die-bonding. Wire bonding, die-bonding. Chip-mounting techniques.	**6**
Total	**40**

Reference books:

1. Hari Singh Nalwa, Handbook of Nanostructured Materials and Nanotechnology (Vol. 3)- Electrical Properties, Academic Press, San Diego, USA (2000).
2. Huff, Howard, Into the Nano Era: Moore's Law Beyond Planar Silicon CMOS (Vol. 106), Springer Series in Materials Science, Springer-Verlag Berlin (2009).
3. Marc J. Madou, Fundamentals of Microfabrication: The Science of Miniaturization, 2nd Edition, CRC Press, California, USA (2002).
4. Kostya (Ken) Ostrikov and Shuyan Xu, Plasma-Aided Nanofabrication: From Plasma Sources to Nanoassembly, WILEY-VCH Verlag GmbH & Co. KGaA (Weinheim) (2007).
5. Guozhong Cao, Nanostructures & Nanomaterials Synthesis, Properties G; Z: Applications, World Scientific Publishing Private, Ltd., Singapore (2004).
6. W.R.Fahrner, Nanotechnology and Nanoelectronics – Materials, Devices, Measurement Techniques, SpringerVerlag Berlin, Germany (2006).
7. R. H. J. Hannink and A. J. Hill, Nanostructure control of materials, Woodhead Publishing Limited and CRC Press LLC, Cambridge, England (2006).
8. Zheng Cui, Nanofabrication, Principles, Capabilities and Limits, Springer Science + business media, New York (2008).

2MVL1-06: FPGA Design Lab

Modelling and Functional Simulation, synthesis and implementation on FPGA of the following digital circuits using Verilog Hardware Description Language

1. Part – I Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor,Multipliers, Decoders, Address decoders, parity generator, ALU
2. Part – II Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters,Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder /Decoder.
3. Part – III Memories and State Machines: Read Only Memory (ROM), Random AccessMemory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers usingFSMs.
4. Part-IV Implementation of UART/Mini Processors on FPGA/CPLD.

2MVL1-07: Advanced VLSI Design Lab

Session-I: VLSI System Design
Design/Simulation and Analysis of following Analog building blocks:

1. Comparators
2. Oscillators
3. PLLs
4. switched capacitor circuits

Session-II: ASIC Design
Experiments shall be carried out using Mentor Graphics/Cadence Tools High Speed/Low Power CMOS Design

1. Designing of combinational/sequential CMOS circuits for High Speed
2. Designing of combinational/sequential CMOS circuits for Low Power

Session III: (Implementation of any one)

1. Non-pipelined MIPS Processor
2. Pipelined MIPS Processor
3. Out of Order Execution with Tomasulo's Algorithm
4. Communication Controllers
5. Arithmetic Circuits
6. DSP Systems

2MVL4-50: MINI PROJECT WITH SEMINAR
2MVL8: AUDIT COURSE 1

Please refer Annexure I

Semester III

3MVL2-11: Nano-Scale Devices: Modeling and Circuits

Syllabus:

CONTENTS	CONTACT HOURS
MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multi-gate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter sub-band scattering, multi-gate technology – mobility – gate stack.	**9**
MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two-dimensional confinement, scattering – mobility.	**9**
Silicon nanowire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for nondegenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors. Radiation effects in SOI MOSFETs, total ionizing dose effects – single-gate SOI – multi-gate devices, single event effect, scaling effects.	**12**
Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.	**10**
Total	**40**

Reference books:

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modeling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000.

3MVL2-12: RF VLSI Circuits

Syllabus:

CONTENTS	CONTACT HOURS
Basic concepts in RF design: Units in RF Design, time variance - Effects of Nonlinearity, - harmonic distortion, gain compression, crossmodulation, intermodulation,cascaded nonlinear stages, AM/PM conversion Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, noise models for active and passive components.	**10**
High frequency amplifier design: Zeros as bandwidth enhancers, shunt-series amplifier, f T doublers, neutralization and uni-lateralization.	**6**
Low noise amplifier design: LNA topologies, power constrained noise optimization, linearity and large signal performance.	**6**
Mixers: Multiplier-based mixers, subsampling mixers, diode-ring mixers. Oscillators & synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.	**10**
RF power amplifiers: Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.	**8**
Total	**40**

Reference books:

1. T.homas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 2nd ed., Cambridge, UK: Cambridge University Press, 2004.
2. B.Razavi, “RF Microelectronics”, 2nd Ed., Prentice Hall, 1998.
3. Abidi, P.R. Gray, and R.G. Meyer, eds., “Integrated Circuits for Wireless Communications”, New York: IEEE Press, 1999.
4. R. Ludwig and P. Bretchko, “RF Circuit Design, Theory and Applications”, Pearson, 2000.
5. Mattuck,A., “Introduction to Analysis”, Prentice-Hall,1998.
6. Recent literature in RF Circuits.

3MVL2-13: Testing of VLSI Circuits

Syllabus:

CONTENTS	CONTACT HOURS
BASICS OF TESTING AND FAULT MODELING: Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling - Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation.	**8**
TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS: Test generation basics - test generation algorithms - path sensitization - Boolean difference – algorithmPODEM - Testable combinational logic circuit design.	**8**
TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS: Testing of sequential circuits as iterative combinational circuits - state table verification – test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan.	**10**
MEMORY, DELAY FAULT AND IDDQ TESTING: Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults – Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing.	**8**
BUILT-IN SELF-TEST: Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.	**6**
Total	**40**

Reference books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.
2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory andMixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. N.K. Jha and S.G. Gupta, “Testing of Digital Systems”, Cambridge University Press.
4. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models andArchitectures”, Springer.

3MVL4-60: Dissertation phase 1: Industrial Project

Please refer Annexure II

SEMESTER IV

4MVL4-70: Dissertation phase II

Please refer Annexure II

ANNEXURE II

(Dissertation)
3MLV4-60: Dissertation Phase – I
3MLV4-70: Dissertation Phase – II

Syllabus Contents:

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have thefollowing

- Relevance to social needs ofsociety
- Relevance to value addition to existing technologies & advancement in theinstitute
- Relevance to industry.
- Problems of nationalimportance
- Research and development in variousdomainthe student should complete thefollowing:
  - Literature survey ProblemDefinition
  - Motivation for study and Objectives
  - Preliminary design / feasibility / modularapproaches
  - Implementation andVerification
  - Report andpresentation

The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification / Proof ofconcept.
- Design, fabrication, testing of CommunicationSystem.
- The viva-voce examination will be based on the above report andwork.

Guidelines for Dissertation Phase – I and II

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January toJune.
- The dissertation may be carried out preferably in-house i.e. department's laboratories and centers OR in research lab/ industry allotted through department's/T & Pcoordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. Thereferred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits- Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective

specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.

- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
- Phase – II evaluation: Guide along with the university appointed examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.