Course: Digital Electronics Circuits

Course Code: noc19-ee09

Session: 2018-19

Duration: 12 Weeks

Assessment procedures: Weekly Assignment (25%) + proctored certification Exam (75%)

Curriculum of the Course:

Week 1: Introduction; Relation between switching and logic operation; Use of Diode and Transistor as switch; Concept of noise margin, fanout, propagation delay; TTL, Schottky TTL, Tristate; CMOS Logic, Interfacing TTL with CMOS

Week 2: Basic logic gates, Universality of NAND, NOR gates, AND-OR-Invert gates, Positive and Negative Logic; Boolean Algebra axioms and basic theorems; Standard and canonical representations of logic functions, Conversion between SOP and POS; Simplification of logic functions, Karnaugh Map, Don't Care Conditions

Week 3: Minimization using Entered Variable Map, Minimization using QM algorithm; Cost criteria, Minimization of multiple output functions; Static-0, Static-1 and Dynamic Hazards and their cover.

Week 4: Multiplexer; Demultiplexer / Decoder, BCD to 7-segment decoder driver; Encoder, Priority encoder; Parity generator and checker

Week 5: Number systems-binary, Signed binary, Octal, hexadecimal number; Binary arithmetic, One's and two's complements arithmetic; Codes, Code converters; Adder, Subtractor, BCD arithmetic

Week 6: Carry look ahead adder; Magnitude comparator; ALU; Error detecting and correcting codes

Week 7: Bistable latch, SR, D, JK, T Flip-Flop: level triggered, edge triggered, master – slave, Various representations of flip-flops; Analysis and synthesis of circuits that use flip-flop

Week 8: Register, Shift register, Universal shift register; Application of shift register: ring counter, Johnson counter, sequence generator and detector, serial adder; Linear feedback shift register

Week 9: Up and down counter, Ripple (asynchronous) counters, Synchronous counters; Counter design using flip flops, Counter design with asynchronous reset or preset; Applications of counters

Week 10: Design of synchronous sequential circuit using Mealy model and Moore model: state transition diagram, algorithm state machine (ASM) chart; State reduction technique

Week 11: Digital to analog converters: weighted resistor/converter, binary ladder, converter, accuracy and resolution; Analog to digital converter: quantization and encoding, different types of conversion, accuracy and resolution

Week 12: Memory organization and operation, Memory expansion; Memory cell; Different types of memory, ROM, PROM, PAL, PLA, CPLD, FPGA

List of students enrolled

S. No	Name of Student
1	Shankar Sharma
2	Shivani Priyadarshani
3	Aadarsh Singh

4	Aditya Choudhary
5	Aditya Kabra
6	Tarun
7	Deepak Agrawal
8	Akshat Gupta
9	Ananya Tiwari
10	Aniket Rathi
11	Anjali Jain
12	Anjali Parik
13	Anjali Gupta
14	Anmol Bajaj
15	Ansh Garg
16	Rohit Arora
17	Brij Bhushan
18	Chetan Sharma
19	Darshan Sharma
20	Deepika Kerwal
21	Falguni Sharma
22	Gargi Sharma
23	Gaurav Hotwani
24	Himanshu Bairwa
25	Hitesh Bhojwani
26	Divyansh Jain
27	Rishika Jain
28	Madhulika Jain
29	Himanshu Jain
30	Jitisha S. Gupta
31	Kanak Agrawal
32	Rishi Maheshwari
33	Kunal Chaudhary
34	Manish Faujdar
35	Yashaswi Mathur
36	Mayur Sharma
37	Aayushi Meena
38	Nikita Modi
39	Monalisa
40	Neha
41	Sachin
42	Saumya Pancholi
43	Ashish Kumar Pathak
44	Pragya Jain
45	Prerna Verma
46	Priya Gupta
47	Rahul Mangal
48	Rahul Saini
49	Rajat Jangid
50	Ritik Kala
51	Sachin Olkha
52	Rajkumar Saini
53	Sanskar Sonkhiya
54	Chinmay Sharma
55	Utkarsh Sharma
56	Shrayansh
57	Shweta Mittal
58	Chatrapal Singh Shaktawat
59	Shikha Singh
60	Subhash Dudi
61	Sushobhit Nigam
62	Shivang Tiwari
63	Vijay
64	Avi Vanawat
65	Rajat Verma
66	Yash Pagariya