Course: CMOS Digital VLSI Design

Course Code: noc21-ee09

Session: 2020-21

Duration: 12 Weeks

Assessment procedures: Weekly Assignment (25%) + proctored certification Exam (75%)

Curriculum of the Course:

MOS Transistor Basic-I; L2: MOS Transistor Basic-I; L3: MOS Transistor Basic-II; L4: MOS Parasitic & SPICE Model; L5: CMOS Inverter Basics-I CMOS Inverter Basics-II; L2: CMOS Inverter Basics-III; L3: Power Analysis-I; L4: Power Analysis-II; L5: SPICE Simulation-I SPICE Simulation-II; L2: Combinational Logic Design-I; L3: Combinational Logic Design-II; L4: Combinational Logic Design-III; L5: Combinational Logic Design-IV Combinational Logic Design-V; L2: Combinational Logic Design-VI; L3: Combinational Logic Design-VII; L4: Combinational Logic Design-VIII; L5: Combinational Logic Design-IX Combinational Logic Design-X; L2: Logical Efforts-I; L3: Logical Efforts-II; L4: Logical Efforts-III; L5: Sequential Logic Design-I Sequential Logic Design-II; L2: Sequential Logic Design-III; L3: Sequential Logic Design-IV; L4: Sequential Logic Design-V; L5: Sequential Logic Design-VI Sequential Logic Design-VII; L2: Sequential Logic Design-VIII; L3: Clocking Strategies for Sequential Design-I; L4: Clocking Strategies for Sequential Design II; L5: Clocking Strategies for Sequential Design-III Clocking Strategies for Sequential Design-IV; L2: Sequential Logic Design-IX; L3: Clocking Strategies for Sequential Design V; L4: Concept of Memory & its Designing-I; L5: Concept of Memory & its Designing-II

List of students enrolled

S. No	Name of Student
1	Rakshita Agarwal
2	Archit Bajpai
3	Ashima Mehta
4	Faisal Khan
5	Rashi Kinra
6	Manisha Balani
7	Monalisa
8	Parul Jain
9	Rashi Sharma
10	Ritik Khandelwal
11	Saumya Gautam
12	Shivansh Dosi
13	Suraj Sharma
14	Ujala Jhanwar
15	Vibhu Mathur
16	Vishal Sen
17	Yash Gaur