Course: System Design Through VERILOG

Course Code: noc21-ee97

Session: 2020-21

Duration: 8 Weeks

Assessment procedures: Weekly Assignment (25%) + proctored certification Exam (75%)

Curriculum of the Course:

Week 1:
- Introduction to Verilog

Week 2:
- Gate level modelling

Week 3:
- Behavioral modelling I

Week 4:
- Behavioral modelling II

Week 5:
- Data flow modelling

Week 6:
- Switch level modelling

Week 7:
- Synthesis of combinational logic using verilog

Week 8:
- Synthesis of sequential logic using verilog

List of students enrolled

S. No	Name of Student
1	Bhumika chhipa
2	Pooja Choudhary
3	Suraj sharma
4	Udyan Srivastava
5	Vipul Gupta
6	Vinayak gupta