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Design and Device Characteristic Analysis of A Triple Material Double Gate (TMDG) Strained Channel MOSFET

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Abstract: **In this paper A Triple Material Double Gate (TMDG) n-MOSFET with strained Si (s-Si) channel is proposed. The proposed MOSFET consist of two gate electrodes. Both gate electrodes have three materials with different work-functions. Channel region of MOSFET has strained Si to enhance mobility of charge carriers. Using ATLAS, which is a 2 dimensional device simulator, we have extracted threshold voltage (V_{th}) of proposed device along with DG MOSFET and DG strained Si channel MOSFET from transfer characteristics of MOSFETs. Trans-conductance (g_m) and DIBL analysis of the MOSFET structures is also done in this paper. The strain in Si channel affects effective mass and inversion layer mobility of electrons of Channel which leads to increased drain current. In DG strained MOSFET, As compared to DG MOSFET, improvement in current is observed but the threshold voltage (V_{th}) of the MOSFET reduces and also DIBL is increased. Reduced threshold voltage is a short channel effect (SCE) which takes place due to reduced potential barrier between source and drain in nanometer regime. TMDG structure leads to increased threshold voltage because of surface potential profile modifications. Surface potential profile of TMDG MOS shows two steps due to three materials used in both the gate electrodes, as a result drain conductance reduces. Reduced drain conductance leads to reduced SCEs like DIBL and Vth lowering. Maximum electric field at the drain electrode also reduces in TMDG structure which minimizes HCE. Threshold voltage also increases in the proposed structure as compared to DG strained MOSFET. Surface potential profile, threshold voltage (V_{th}), trans-conductance (g_m) and DIBL variation are observed in TMDG s-Si n-MOSFET. Proposed MOS device incorporates advantages of both TMDG MOS and strained Si channel MOSFET device to increase performance of high density chips in MOS VLSI technology.**

Keywords- DG MOSFET, TMDG MOSET, Strained-Si Channel, trans-conductance (g_m), Surface Potential Profile

I. INTRODUCTION

As MOSFETs physical dimensions have reached in sub nano-meter regime due to scaling of transistors, manufacturing limits impede further scale down of transistors. So Innovation in structure of MOSFETs and materials used is required for performance improvements and further miniaturization of MOSFETs[1].Use of Multiple gates and multiple material in gate electrode of MOS devices is the prominent way to get rid of the Short channel effects (SCEs) like DIBL and HCE. These effects (SCEs) occurring from downscaling of MOSFET's physical dimensions are effectively minimized in the proposed structure, which is a Triple Material Double Gate (TMDG) NMOS with strained Si (s-Si) channel, as compared to conventional Double Gate MOSFET and DG strained channel MOSFET.

A. Triple Material Double Gate (TMDG) MOS Devices

Triple Material Double Gate (TMDG) MOSFETs integrates benefits of both triple material gate MOSFETs and double gate MOSFETs. In double gate MOSFET structures, the effective controlling of gate increases because of the channel inversion layer formed into the whole silicon channel. Therefore, MOS shows higher saturation current and lower leakage current performance. In short channel MOSFETs due to high lateral electric field drift velocities of majority carriers saturates which reduces control of gate voltage(V_{gs}) over drain current and sub-threshold conduction takes place in MOSFET[8].This effect is minimized by the use of multiple materials in gate. Proposed MOSFET structure has two symmetric gate electrodes. Both upper and lower gate has three materials of different work-functions Φ_{m1}, Φ_{m2} and Φ_{m3} deposited over equal lengths. Material work-functions are selected such that the work-function of material which is towards the source is maximum and material work-function towards drain is minimum (i.e. $\Phi_{m1} > \Phi_{m2} > \Phi_{m3}$) in both gate electrodes. High work-function near the source accelerates charge carriers more rapidly and lower work-function towards the drain minimizes electric field peak at drain side that suppresses DIBL and other effects which are generated due to short geometries.

B. Strained Si Channel Devices

In short channel MOSFET devices, To sustain a smaller electric field in the channel region, and non-overlapping of depletion layers of source and drain electrodes, need of high doping becomes necessary. But a severe effect of reduction in mobility comes in picture with high doping concentration in channel region [7]. Also high vertical field influences the scattering of carriers in the surface region so the surface mobility of carriers is reduced with respect to bulk mobility [8].The mobility of charge carriers is increased using a technique strain technology (Mobility enhancement technology). Strained-Si channel MOSFETs shows around 70% higher effective mobility μ_{eff} than mobility of the charge carriers in unstrained Si channel [8].

1) Effect of Strain: Strain is deformation of atomic structure of a material, when a thin layer of silicon is deposited over relaxed $Si_{1-x}Ge_x$ substrate, Si feels some biaxial tension or strain due to mismatch in lattice constant. Due to this biaxial strain, the electron affinity of silicon increases as a result band-gap and effective mass of the charge carriers in Si decreases. As a consequence of all these

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