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An investigation on a triple material double gate cylindrical gate all around (TMDG-CGAA) MOSFET for enhanced device performance

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ABSTRACT

The present work investigates the Triple Material Double Gate Cylindrical Gate All Around (TMDG-CGAA) MOSFET in the nanometer regime to improve the device performance. Electrical parameters of TMDG-CGAA MOSFET are investigated under varying physical conditions like channel length, channel thickness, oxide thickness, and core diameter. For various parameters like drain current, threshold voltage, DIBL, and transconductance the TMDG-CGAA MOSFETs are evaluated. The comparison has been done among the SG-CGAA MOSFET, DG-CGAA MOSFET, and TMDG-CGAA MOSFET by using the same device parameters. The proposed structure TMDG-CGAA MOSFET has been validated by a device simulator named as 3D ATLAS tool. The device performance enhances by incorporating three materials at the gate electrode in the DG-CGAA MOSFET. In the planar MOSFET devices the SCEs enhances and also the threshold voltage is rolling off due to the reduced potential barrier between source and drain. But in the proposed structure the threshold voltage increases in the nanometer region also due to its cylindrical geometry. The drain current, transconductance also improves in comparison with the SG-CGAA MOSFET and DG-CGAA MOSFET. The SCE like DIBL decreases in the proposed structure. So overall the proposed structure shows better device performance with fast switching and lower cost.

1. Introduction

Continuous downscaling of the MOSFETs are necessary to get higher packaging density and higher speed of the circuit. But short channel effects like Drain Induced Barrier Lowering (DIBL), Hot Carrier Effects (HCE), and threshold voltage roll-off, etc, rise by the continuous shrinking of the MOSFETs. Under sub-30 nm further downscaling of the device is not possible. Because the threshold voltage rolled off and SCEs rise. So new technologies and materials are required along with the new non-conventional geometries of the MOSFETs. New MOSFET structures from SOI to Multigate devices are used to reduce the SCEs. Multigate devices are Double gate (DG) MOSFETs, tri-gate (pi-gate and omega-gate) MOSFET, quadruple gate (Quad-gate) MOSFET and gate all around (GAA) MOSFETs.The electrostatic integrity and the gate control over the channel increases in the multigate devices [1–4]. The highest SCE immunity is shown in the Gate All Around (GAA) devices among all the multigate devices because the gate is wrapped around the channel region so the gate controllability enhances and SCEs reduces [5]. By combining the gate engineering and the material engineering the device performance can be further enhanced under the nanometer regime also.

Cylindrical and rectangular-shaped geometries are used in the Gate All Around structure. In the rectangular GAA, the gate is wrapped around the rectangular-shaped channel region and in the Cylindrical Gate All Around (CGAA) devices, the gate is wrapped around the cylindrically shaped channel region. In both devices, the immunity towards the SCEs enhances but in the rectangular GAA devices corner effects arise [6], by which the device performance degraded in the rectangular devices. In the CGAA devices corner effects reduces and the device performance increases. In the CGAA devices, SCEs like DIBL, threshold voltage roll-off reduces and transconductance increases. But the on-current delivered in the multigate devices is reduced. The

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