Hands-on training and workshop on Xilinx Vivado VLSI EDA tool and FPGA trainer kits.10-11 April 2018

1. **Title of the activity:** Hands-on training and workshop on Xilinx Vivado VLSI EDA tool and FPGA Trainer Kits
2. **About the activity:-**
   a. **Objective of Workshop:**

Main Objective was to provide hands on knowledge in Digital VLSI using FPGA board. This workshop provides the participants with an introduction to digital design tool flow in Xilinx programmable devices (PLDs) using Vivado Design software suite. The program will focus on practical aspects and include examples which are relevant to the current industry requirements. Lab sessions will include the following:

• Digital Design concepts.
• FPGA design flow using Vivado.
• Block Memory implementation in vivado.
• FSM implementation in Vivado & XSIM simulation
• Vivado logic analyzer & its features
• Introduction to HLS
• Optimizing for Area and Resources

b. Expected Outcome of Workshop:

Participant will be able to get the hands on knowledge of Digital VLSI design flow on FPGA boards using Xilinx Vivado EDA tool.

Other Outcomes of the event

(a) Benefits to Faculties

- Faculty Skill Development: Faculties gains valuable information regarding different stages of VLSI, XILINX (Vivado), HDL that improve their teaching quality, content etc.
- Participants got more practical exposure to the digital circuit design.
- They can demonstrate knowledge and understanding of the tool and carry out research in different areas of VLSI resulting in publications and product development.
- Helpful in achieving the course outcomes of different VLSI courses like VHDL, VERILOG.

(b) Benefits to Students

- After completion of workshop students will be able to

- Design and develop innovative projects in the field of VLSI.
- Recognition of the need for, and an ability to engage in life-long learning.

(c) Duration – 10 to 11 April, 2018 (Two Days)

(d) Venue – M. Tech. Lab (ECL-06), ECE Deptt.

e. Type of Workshop – National

3. Details of the activity:

a. External Resource Person:

S. No.	Name	Organization	Country
1	Mr. Ankur Sangal	Senior Application Engineer, CoreEL Technologies (I) Pvt. Ltd., Delhi	India

b. Number of participants: 22

Faculties/ Participants: 14

Faculty/ Participants List

1) Dr. Swati Arora
2) Mamta Jain
3) Vikas Pathak
4) Pooja Choudhary
5) Neeraj Jain
6) Rahul Pandey
7) Manju Choudhary
8) Priyanka Sharma
9) Namrata Joshi
10) S. Sarabjeet Singh
11) Shanu Tripathi
12) Ashish Sharma
13) Abhilasha Yadav
14) Suman Sharma

Students List: 8

1) Yogesh Soni
2) Yamini Rathore
3) Harshit Mathur
4) Divya Rahtore
5) Ankita Sharma
6) Ashmita Menariya
7) Ila Roy
8) Vivek Jaimini

c. Attainment of the Objective:

The objective and outcome of workshop is successfully achieved by all participants.

d. Brief proceedings of each day of the activity:

Day 1:

- 7-Series Architecture Overview
- **Lab 1: Vivado Design Flow**
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.
- Synthesis Technique
- **Lab 2: Synthesizing a RTL Design**
  - Synthesize a design with the default settings as well as other settings changed and observe the effect.
- Implementation and Static Timing Analysis
- **Lab 3: Implementing the Design**
  - Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.

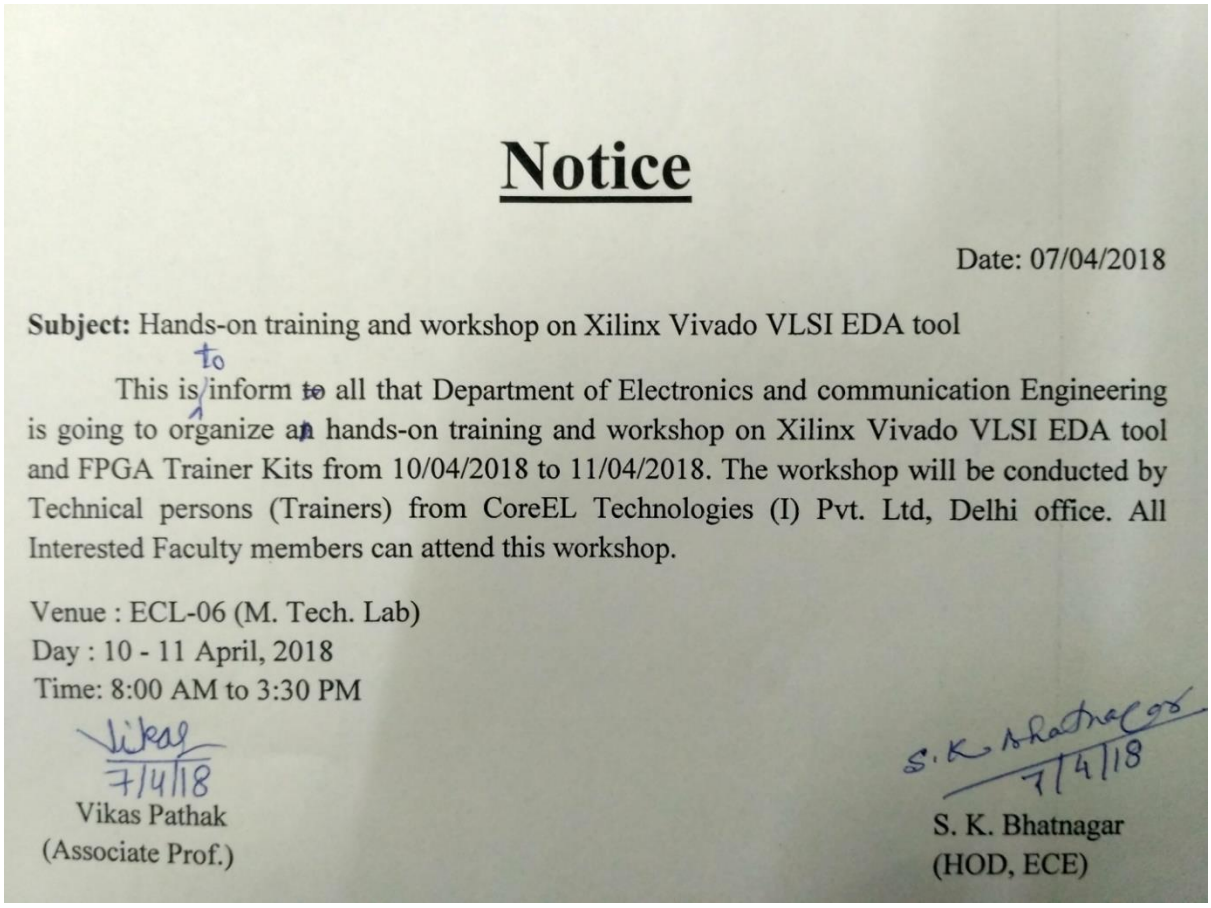
Day 2:

- IP Integrator
- **Lab 4: Using the IP Catalog and IP Integrator**
  - Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.
- Xilinx Design Constraints
- **Lab 5: Xilinx Design Constraints**
  - Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the timing analysis.
- Hardware Debugging
- **Lab 6: Hardware Debugging**
  - Use Mark Debug feature and also available Integrated Logic Analyzer (ILA) core (available in IP Catalog) to debug the hardware.

4. Enclosures:-

a. Workshop Notice
b. Attendance of Participants
c. Feedback form of participants

Workshop Notice



Notice

Date: 07/04/2018

Subject: Hands-on training and workshop on Xilinx Vivado VLSI EDA tool

This is to inform all that Department of Electronics and communication Engineering is going to organize a hands-on training and workshop on Xilinx Vivado VLSI EDA tool and FPGA Trainer Kits from 10/04/2018 to 11/04/2018. The workshop will be conducted by Technical persons (Trainers) from CoreEL Technologies (I) Pvt. Ltd, Delhi office. All Interested Faculty members can attend this workshop.

Venue : ECL-06 (M. Tech. Lab)
Day : 10 - 11 April, 2018
Time: 8:00 AM to 3:30 PM

Vikas
7/4/18
Vikas Pathak
(Associate Prof.)

S. K. Bhatnagar
7/4/18
S. K. Bhatnagar
(HOD, ECE)

Attendance of Participants

CoreEL Technologies

Institution Name :- **Swami Keshvanand Institute of Technology, Jaipur**

TRAINING/Installation on: - **Vivado Design Suite with Nexys 4 DDR & Zybo**

No of days: **02 Days**

CoreEL Trainer: --- --**ANKUR SANGAL** ---------------signature-------------------

DATE: - ---from----- **10/04/2018** ----------------to-------------**11/04/2018** ------

Venue: ------**ECE Department, SKIT Jaipur**---

FACULTY IN CHARGE OF INSTITUITION: - Vikas Pathak signature------

DEPARTMENT: --------ECE---seal---------------------

NAME OF PARTICIPANT / College Name	Email id	Contact number	Feedback 1-10 (10 being highest)	Signature
NAMRATA JOSHI	namrita.in@gmail.com	9982154678	10	Namrata
SHANU TRIPATHI	shanu.tripathi@skit.ac.in	8209414895	10	Shanu
Mamta Jain	ermamta@yahoo.co.in	9772740951	09	Mamta
Pooja choudhary	poojachoudhary87@gmail.com	9460869377	10	Pooja
Manju Choudhary	manjuchoudharymec@gmail.com	7694724109	10	Manju
Abhilasha Yadav	abhilasha852@gmail.com	9891887276	10	Abhiyad
Swati Arora	aroraswati14@gmail.com	9982036051	09	[illegible]
Neeraj Jain	neerajengi24@gmail.com	9468666815	09	[illegible]
S. Sarabjeet Singh	ece_sarabjeet@yahoo.co.in	9828785582	07	Singh
Vikas Pathak	vikaspathak85@gmail.com	8503856191	09	Vikas
Ashish Sharma	ashishsharma.skit@gmail.com	9694945550	10	Ashish

CoreEL Technologies (India) Pvt Ltd.
21,7TH MAIN I BLOCK KORAMANGALA
BANGALORE-560034

CoreEL Technologies

Priyanka Sharma	priyanka-vlsi@gmail.com	810793--8391	09	Priyanka
Rahul Pandey	rahul.ec.29@gmail.com	7073903153	08	Rahul
YOGIESH SONI	yogeshsoni110@gmail.com	9680117686	09	Yogesh
Vivek Jaimini	vivekjaimini11@gmail.	8952011014	08	Vivek
DIVYA RATHORE	divya-rathore28@yahoo.com	9462728991	08	Divya
ASMITA Menariya	ashu.menariya@gmail.com	8769124508	08	Asmita
ANKITA SHARMA	ankit1988@yahoo.com	7073083683	09	Ankita
Ila Roy	illeroy611@gmail.com	02598242119	09	Ila Roy

CoreEL Technologies (India) Pvt. Ltd.
21,7TH MAIN I BLOCK KORAMANGALA
BANGALORE-560034

Feedback form of participants

Hands-on training and workshop

on

Xilinx Vivado VLSI EDA tool

10 and 11 April 2018

Feedback Form

Name of Participant: .....

Teaching Experience: .....

1) What is your overall assessment of the workshop? (1 = insufficient - 5 = excellent)

1 2 3 4 5

2) Which topics or aspects of the workshop did you find most interesting or useful

---

---

3) Did the workshop achieve the programme objectives?

Yes No

4) Knowledge and information gained from participating in this workshop?

Met your expectations Yes No Somehow

5) Will be useful/applicable in my work Definitely Mostly Somehow Not at all

6) How do you think the workshop could have been made more effective?

---

7) Comments and suggestions (including activities or initiatives you think would be useful, for the future?

Signature of Participant

THANK YOU!